S3FN21D

32-BIT CMOS Microcontrollers

Revision 0.00

April 2010

Data Sheet

SAMSUNG ELECTRONICS

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S3FN21D 32-BIT CMOS Microcontrollers
Data Sheet, Revision 0.00

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1 OVERVIEW

S3FN21D is a family of cost-effective and high-performance microcontrollers with Cortex-M0 designed by Advanced RISC Machines (ARM).

- ARM Cortex-M0 Core
- Built-in up to 128 Kbytes Program Flash Memory
- Internal up to 8 Kbytes SRAM for stack and data memory
- Operating temperature: –40 ~ 85°C
- Operating voltage range: 1.8 ~ 5.5V
- Interrupt controller: Dynamically reconfigurable Nested Vectored Interrupt Controller
- USB2.0 Full speed mode support
- LCD Controller / Driver: 32 COM × 80 SEG
- Connectivity: 3 × USART/LIN, 2 × SPI / I2C
- Up to 6 x 16-bit Timers and 2 × 32-bit Timers
- Up to 12 channels of 10-bit ADC
- Watch-Dog Timer
- Crystal/Ceramic oscillator or external clock can be used as the clock source and PLL
- Low Power Modes: Sleep and Idle

1.1 FEATURES

CPU

- 32-bit RISC ARM Cortex-M0 Core
- SWD Debugging Solution

Memory

- Program Memory (Full Flash ROM)
  - 128KB program memory
  - Internal flash memory (Program memory)
    - 10 Years data retention
    - User program and sector erase available
    - Endurance: 10,000 erase/program cycles
    - External serial programming support
- Data Memory (RAM)
  - 8KB data memory
- LCD Display Memory (RAM)

144 I/O Pins

- I/O: 32 pins (Sharing with other signal)
- I/O: 144 pins (Sharing with LCD signal outputs)

Interrupts

- 32 interrupt vector sources (not including 16 Cortex own interrupt vector sources)

16-Bit Watchdog Timer

- Watchdog timer function
- 4 kinds of clock source

16-Bit Timer/Counter 0, 1, 2, 3, 4, 5

- Programmable 16-bit interval timer
- External event counter function
- PWM and capture function
- Match and overflow mode

32-Bit Timer/Counter 6, 7

- Programmable 32-bit interval timer
- External event counter function
- PWM and capture function
- Match and overflow mode

32-Bit Free Running Timer

- 32-bit free running timer
- Operation in STOP mode with ISCLK

Watch Timer

- Interval time: 3.91mS, 0.125S, 0.25S, and 0.5S at 32.768kHz
- 0.5/1/2/4kHz Selectable buzzer output

PWM 0, 1

- Upto 16-bit programmable PWM
- 6-bit extension

LCD Controller/Driver

- 80 segments and 32 common terminals
- 1/8, 1/12, 1/16, and 1/32 duty selectable
- Capacitor or resistor bias selectable
- Regulator and booster circuit for LCD bias analog to Digital Converter
- 12-channel analog input
- 10-bit conversion resolution
- 25us conversion time
- Dedicated DMA channels

USART-LIN

- 3 channels of USART-LIN (0/1/2)
- Dedicated DMA channels

IIC Bus Interface (I2C)

- 2 channels of Multi-Master IIC-Bus
- Serial, 8-bit Oriented and Bi-directional Data Transfers
- 100Kbit/s in Standard Mode and up to 400Kbit/s in Fast mode
- Dedicated DMA channels

SPI Bus Interface

- 4 to 16-bit Programmable Data Length: SPI0, SPI1
- Support Master and Slave Mode
- Dedicated DMA channels

USB2.0 Full Speed Mode (12MHz) Support

- Integrated bus transceiver
- Support 1 device address and 5 endpoints
- Control, In1/Out1 and In2/Out2 endpoints
- Three 16-bytes and two 64-bytes endpoints
- Each data endpoint is capable of handling bulk, interrupt, and isochronous data transfers
- Dedicated DMA channels

Direct Memory Access (DMA)

- 6 independently configurable channels
- Transfer from Peripheral to Memory
- Transfer from Memory to Peripheral
- Transfer from Memory to Memory

Low Voltage Detection (LVD)

- Reset with configurable voltage level
- Interrupt/Flag with configurable voltage level
- Criteria voltage: 1.7 / 1.9 / 2.1 / 2.6 / 3.8 / 4.3V
- Reset/Interrupt enable/disable can be controllable

Two Power-Down Modes

- Idle: CPU clock (CORECLK) Stops
- Sleep: External Oscillator and Clock to Peripherals Stop

Oscillation Sources

- Crystal, ceramic, or RC for main clock (Internal or external RC oscillation)
- 0.4MHz - 20.0MHz oscillation circuit for main clock
- 32.768kHz crystal oscillation circuit for sub clock
- PLL 12 - 40MHz for main clock
- USB 48MHz by PLL
- 8/16MHz & 20MHz internal main oscillator
- 32.768kHz internal sub-oscillator

LDO

- 3.3V output low dropout regulator for USB IO

Operating Voltage Range

- 1.8V to 5.5V at 0.4 - 4.2MHz
- 2.2V to 5.5V at 0.4 - 12.0MHz
- 2.7V to 5.5V at 0.4 - 40.0MHz

Operating Temperature Range

- –40°C to + 85°C

Package Type

- 176-LQFP

1.2 BLOCK DIAGRAM

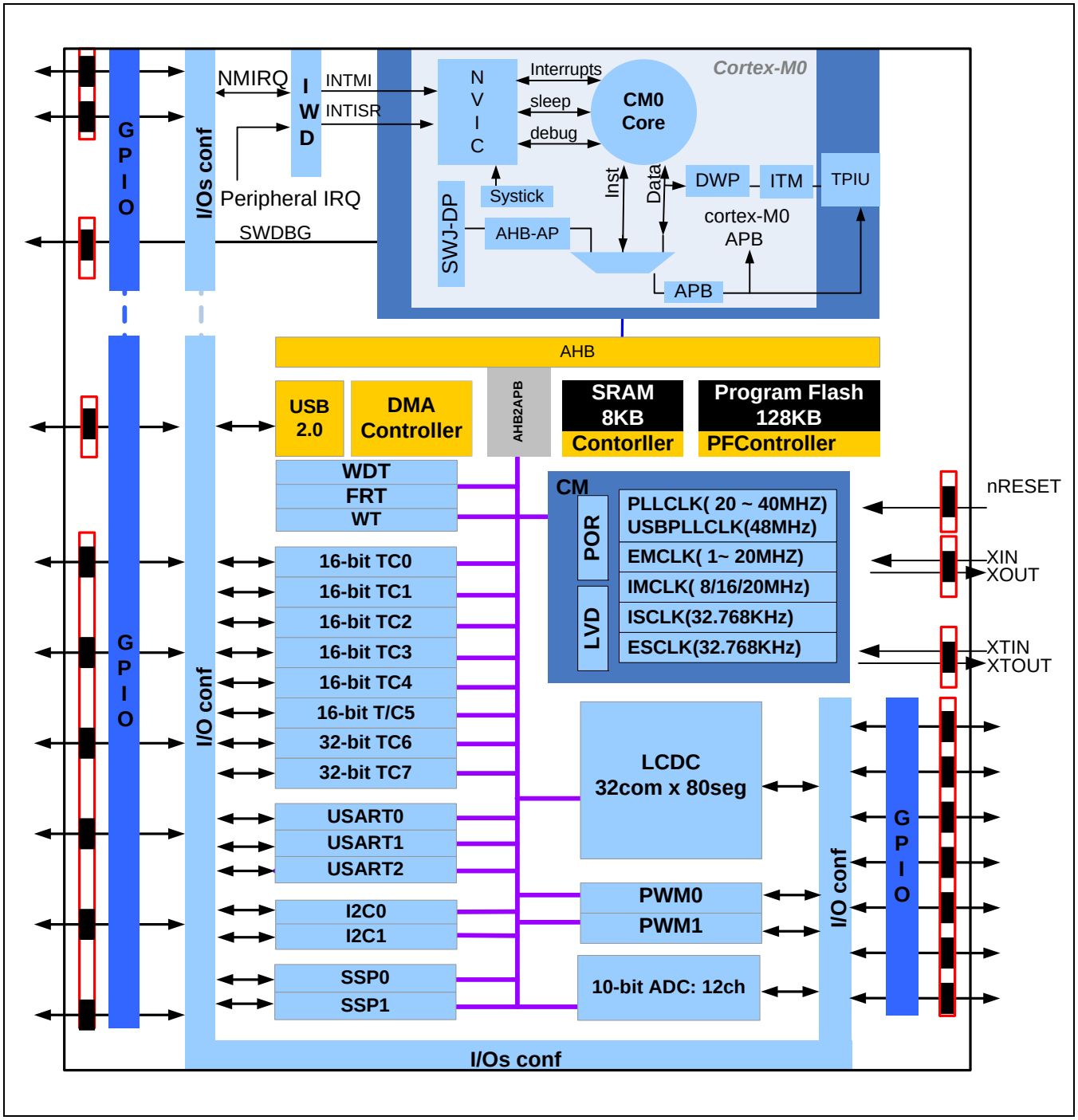

Figure 1-1 Block Diagram

2 PIN CONFIGURATION

2.1 PIN CONFIGURATION

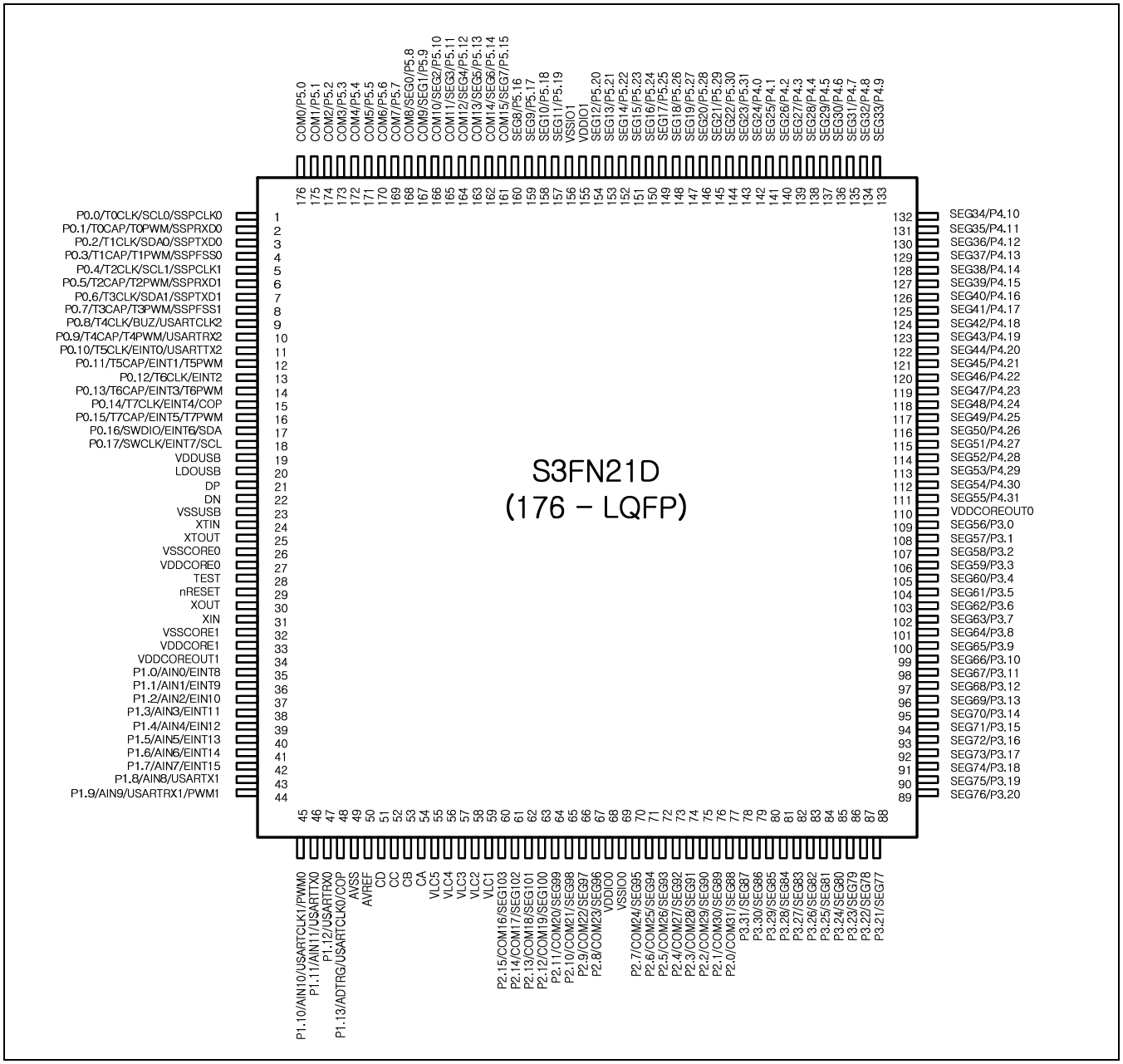

Figure 2-1 Pin Configuration

2.2 PIN ASSIGNMENTS

Table 2-1 Pin Assignments - Pin Number Order

Pin Num.	1st	2nd	3rd	4th	Flash
1	P0.0	T0CLK	SCL0	SSPCLK0	
2	P0.1	T0CAP	T0PWM	SSPRXD0	
3	P0.2	T1CLK	SDA0	SSPTXD0	
4	P0.3	T1CAP	T1PWM	SSPFSS0	
5	P0.4	T2CLK	SCL1	SSPCLK1	
6	P0.5	T2CAP	T2PWM	SSPRXD1	
7	P0.6	T3CLK	SDA1	SSPTXD1	
8	P0.7	T3CAP	T3PWM	SSPFSS1	
9	P0.8	T4CLK	BUZ	USARTTX2	
10	P0.9	T4CAP	T4PWM	USARTRX2	
11	P0.10	T5CLK	EINT0	USARTCLK2	
12	P0.11	T5CAP	EINT1	T5PWM	
13	P0.12	T6CLK	EINT2		
14	P0.13	T6CAP	EINT3	T6PWM	
15	P0.14	T7CLK	EINT4	COP	
16	P0.15	T7CAP	EINT5	T7PWM	
17	P0.16	SWDIO	EINT6		
18	P0.17	SWCLK	EINT7		
19	VDDUSB				
20	LDOOUT				SDA
21	DP	DP	DP	DP	SCL
22	DN	DN	DN	DN	
23	VSSUSB				
24	XTIN	XTIN	XTIN	XTIN	
25	XTOUT	XTOUT	XTOUT	XTOUT	
26	VSSCORE0				
27	VDDCORE0				
28	TEST	TEST	TEST	TEST	
29	nRESET	nRESET	nRESET	nRESET	
30	XOUT	XOUT	XOUT	XOUT	
31	XIN	XIN	XIN	XIN	
32	VSSCORE1				
33	VDDCORE1				
34	VDDCOREOUT1				

Pin Num.	1st	2nd	3rd	4th	Flash
35	P1.0	AIN0	EINT8		
36	P1.1	AIN1	EINT9		
37	P1.2	AIN2	EINT10		
38	P1.3	AIN3	EINT11		
39	P1.4	AIN4	EINT12		
40	P1.5	AIN5	EINT13		
41	P1.6	AIN6	EINT14		
42	P1.7	AIN7	EINT15		
43	P1.8	AIN8	USARTTX1		
44	P1.9	AIN9	USARTRX1	PWM1	
45	P1.10	AIN10	USARTCLK1	PWM0	
46	P1.11	AIN11	USARTTX0		
47	P1.12		USARTRX0		
48	P1.13	ADTRG	USARTCLK0	COP	
49	AVSS				
50	AVREF				
51	CD	CD	CD	CD	
52	CC	CC	CC	CC	
53	CB	CB	CB	CB	
54	CA	CA	CA	CA	
55	VLC5	VLC5	VLC5	VLC5	
56	VLC4	VLC4	VLC4	VLC4	
57	VLC3	VLC3	VLC3	VLC3	
58	VLC2	VLC2	VLC2	VLC2	
59	VLC1	VLC1	VLC1	VLC1	
60	P2.15	COM16/ SEG103			
61	P2.14	COM17/ SEG102			
62	P2.13	COM18/ SEG101			
63	P2.12	COM19/ SEG100			
64	P2.11	COM20/ SEG99			
65	P2.10	COM21/ SEG98			
66	P2.9	COM22/ SEG97			

Pin Num.	1st	2nd	3rd	4th	Flash
67	P2.8	COM23/ SEG96			
68	VDDIO0				
69	VSSIO0				
70	P2.7	COM24/ SEG95			
71	P2.6	COM25/ SEG94			
72	P2.5	COM26/ SEG93			
73	P2.4	COM27/ SEG92			
74	P2.3	COM28/ SEG91			
75	P2.2	COM29/ SEG90			
76	P2.1	COM30/ SEG89			
77	P2.0	COM31/ SEG88			
78	P3.31	SEG87			
79	P3.30	SEG86			
80	P3.29	SEG85			
81	P3.28	SEG84			
82	P3.27	SEG83			
83	P3.26	SEG82			
84	P3.25	SEG81			
85	P3.24	SEG80			
86	P3.23	SEG79			
87	P3.22	SEG78			
88	P3.21	SEG77			
89	P3.20	SEG76			
90	P3.19	SEG75			
91	P3.18	SEG74			
92	P3.17	SEG73			
93	P3.16	SEG72			
94	P3.15	SEG71			
95	P3.14	SEG70			
96	P3.13	SEG69			

Pin Num.	1st	2nd	3rd	4th	Flash
97	P3.12	SEG68			
98	P3.11	SEG67			
99	P3.10	SEG66			
100	P3.9	SEG65			
101	P3.8	SEG64			
102	P3.7	SEG63			
103	P3.6	SEG62			
104	P3.5	SEG61			
105	P3.4	SEG60			
106	P3.3	SEG59			
107	P3.2	SEG58			
108	P3.1	SEG57			
109	P3.0	SEG56			
110	VDDCOREOUT0				
111	P4.31	SEG55			
112	P4.30	SEG54			
113	P4.29	SEG53			
114	P4.28	SEG52			
115	P4.27	SEG51			
116	P4.26	SEG50			
117	P4.25	SEG49			
118	P4.24	SEG48			
119	P4.23	SEG47			
120	P4.22	SEG46			
121	P4.21	SEG45			
122	P4.20	SEG44			
123	P4.19	SEG43			
124	P4.18	SEG42			
125	P4.17	SEG41			
126	P4.16	SEG40			
127	P4.15	SEG39			
128	P4.14	SEG38			
129	P4.13	SEG37			
130	P4.12	SEG36			
131	P4.11	SEG35			
132	P4.10	SEG34			
133	P4.9	SEG33			

Pin Num.	1st	2nd	3rd	4th	Flash
134	P4.8	SEG32			
135	P4.7	SEG31			
136	P4.6	SEG30			
137	P4.5	SEG29			
138	P4.4	SEG28			
139	P4.3	SEG27			
140	P4.2	SEG26			
141	P4.1	SEG25			
142	P4.0	SEG24			
143	P5.31	SEG23			
144	P5.30	SEG22			
145	P5.29	SEG21			
146	P5.28	SEG20			
147	P5.27	SEG19			
148	P5.26	SEG18			
149	P5.25	SEG17			
150	P5.24	SEG16			
151	P5.23	SEG15			
152	P5.22	SEG14			
153	P5.21	SEG13			
154	P5.20	SEG12			
155	VDDIO1				
156	VSSIO1				
157	P5.19	SEG11			
158	P5.18	SEG10			
159	P5.17	SEG9			
160	P5.16	SEG8			
161	P5.15	COM15/ SEG7			
162	P5.14	COM14/ SEG6			
163	P5.13	COM13/ SEG5			
164	P5.12	COM12/ SEG4			
165	P5.11	COM11/ SEG3			
166	P5.10	COM10/ SEG2			
167	P5.9	COM9 / SEG1			
168	P5.8	COM8/ SEG0			
169	P5.7	COM7			
170	P5.6	COM6			

Pin Num.	1st	2nd	3rd	4th	Flash
171	P5.5	COM5			
172	P5.4	COM4			
173	P5.3	COM3			
174	P5.2	COM2			
175	P5.1	COM1			
176	P5.0	COM0			

2.3 PIN DESCRIPTION

2.3.1 FUNCTION PIN

Table 2-2 Pin Description

Module	Pin Name	Function	D/A	I/O	Comments
RESET	nRESET	Hardware Reset Input	D	I	
CM	XIN	External Main Oscillator Input	A	I	
	XOUT	External Main Oscillator Output	A	O	
	XTIN	External Sub Oscillator Input	A	I	
	XTOUT	External Sub Oscillator Output	A	O	
GPIO	P0.[17:0]	General Purpose I/O Multiplexed	D	I/O	Pull-Up resistor, Multiplexed with peripheral module
	P1.[13:0]	General Purpose I/O Multiplexed	D	I/O	
	P2.[15: 0]	General Purpose I/O Multiplexed	D	I/O	
	P3.[31: 0]	General Purpose I/O Multiplexed	D	I/O	
	P4.[31: 0]	General Purpose I/O Multiplexed	D	I/O	
	P5.[31: 0]	General Purpose I/O Multiplexed	D	I/O	
INTERRUPT	EINT[15:0]	External interrupt request 16			
ADC	AIN[11:0]	Analog Input Channels	A	I	
	ADTRG	ADC External Trigger Input Pin	D	I	
16-BIT TIMER	TxCLK[5:0]	External clock input for Timer	D	I	
	TxCAP[5:0]	Capture input for Timer	D	I	
	TxPWM[5:0]	PWM output for Timer	D	O	
32-BIT TIMER	TxCLK[7:6]	External clock input for Timer	D	I	
	TxCAP[7:6]	Capture input for Timer	D	I	
	TxPWM[7:6]	PWM output for Timer	D	O	
PWM	PWM[1:0]	Pulse width modulation output	D	O	
WT	BUZ	Buzzer Output	D	O	
LCDC	COM[7:0]	COM Driver Signal Pin	D	O	
	COM[15:8]/SEG[7:0] COM[31:16]/SEG[88:103]	COM/SEG Driver Signal Pin			

Module	Pin Name	Function	D/A	I/O	Comments
	SEG[87:8]	SEG Driver Signal Pin	D	O	
	VLC[5:1]	LCD Operating Power Supply Pin	A		
	CA, CB, CC, CD	Capacitor Terminal for Voltage Booster	A		
USART	USARTRX[2:0]	Received Signal Input	D	I	
	USARTTX[2:0]	Transmit Signal Output	D	O	
	USARTCLK[2:0]	Clock Signal	D	I/O	
SPI	SSPCLK[1:0]	SPI Clock	D	I/O	
	SSPRXD[1:0]	Master In Slave Out	D	I/O	
	SSPTXD[1:0]	Master Out Slave In	D	I/O	
	SSPFSS[1:0]	Peripheral Chip Select	D		
I2C	SDA[1:0]	Serial data	D	I/O	
	SCL[1:0]	Serial clock	D	I/O	
USB	DP	USB Data+	A		
	DN	USB Data-	A		
DEBUG	SWDIO	Test Mode Select/ Serial Wire Data Input Output	D	I/O	Internal pull-up
	SWCLK	Test Clock/ Serial Wire Clock	D	I	
MODE	TEST	Test Reserved Pin (2)	D	I	Internal pull-down
FLASH	SDA	Serial Data pin (Output when reading, Input when writing)		I/O	
	SCL	Serial Clock		I	

NOTE:

1. D: Digital, A: Analog, I/O: Input and Output (Bi-direction), O: Output, I: Input
2.

TEST	Mode Setting
0	User Normal/Debug Mode
1	User Flash Writing Tool Mode / Test Mode

Table 2-3 Power Pin Description

Module	Pin Name	Function Description	Comments
Power	VDDCORE[1:0]	Core DC Supply Voltage	
	VSSCORE[1:0]	Core Ground	
	VDDCOREOUT[1:0]	Core Regulator Output	
	VDDIO[1:0]	I/O DC Supply Voltage	
	VSSIO[1:0]	I/O Ground Voltage	–
	AVREF	ADC Reference Voltage	See recommended operating condition
	AVSS	ADC Ground Voltage	–
	LDOUSB	LDO 3.3V Output	
	VDDUSB	USB Supply Voltage	
	VSSUSB	USB Ground	

3 SYSTEM MEMORY MANAGEMENT

3.1 DEFAULT MEMORY MAP

The S3FN21D has memory space allocation as below.

Table 3-1 S3FN21D Memory Map

Address	Memory
Reserved	Reserved
0xE00F_FFFF ~ 0xE000_0000	Cortex-M0 internal peripheral registers
Reserved	Reserved
0x4011_FFFF ~ 0x4000_0000	Special function registers
Reserved	Reserved
0x2000_1FFF ~ 0x2000_0000	8Kbytes internal SRAM memory
Reserved	Reserved
0x0001_FFFF ~ 0x0000_0000	128 Kbytes internal program Flash memory

3.2 SPECIAL FUNCTION REGISTER MAP

3.2.1 CORE SPECIAL FUNCTION REGISTER MAP

Table 3-2 Core Special Function Register Map

Base Address	Peripheral	Description
0xE00F_F000	ROM Table	ROM memory table
0xE004_2000	External PPB	Private Peripheral Bus
0xE004_0000	TPIU	Trace Port Interface
0xE000_F000	Reserved	-
0xE000_E000	SCS	System Control Space
0xE000_3000	Reserved	-
0xE000_2000	FPB	Flash Patch & Break Pint
0xE000_1000	DWT	Data Watch Point & Trace
0xE000_0000	ITM	Instrumentation Trace Macro-cell

3.2.2 PERIPHEAL SPECIAL FUNCTION REGISTER MAP

Table 3-3 Peripheral Memory Map

	Base Address	Peripheral	Description
USB	0x4011_0000	USB	USB Controller
DMAC	0x4010_0000	DMAC	Direct Memory Access Controller
LCDC	0x400D_0000	LCDC	LCD Controller
WT	0x400C_0000	WT	Watch Timer
I2C	0x400A_1000	I2C1	Inter-integrated Circuit 1
	0x400A_0000	I2C0	Inter-integrated Circuit 0
SPI	0x4009_1000	SPI1	Serial Peripheral Interface 1
	0x4009_0000	SPI0	Serial Peripheral Interface 0
USART	0x4008_2000	USART2	Universal Asynchronous Receiver/Transmitter 2
	0x4008_1000	USART1	Universal Asynchronous Receiver/Transmitter 1
	0x4008_0000	USART0	Universal Asynchronous Receiver/Transmitter 0
PWM	0x4007_1000	PWM1	Pulse Width Modulation 1 (16bit)
	0x4007_0000	PWM0	Pulse Width Modulation 0 (16bit)
TIMER / COUNTER	0x4006_7000	TC7	Timer/Counter 7 (32-bit)
	0x4006_6000	TC6	Timer/Counter 6 (32-bit)
	0x4006_5000	TC5	Timer/Counter 5 (16-bit)
	0x4006_4000	TC4	Timer/Counter 4 (16-bit)
	0x4006_3000	TC3	Timer/Counter 3 (16-bit)
	0x4006_2000	TC2	Timer/Counter 2 (16-bit)
	0x4006_1000	TC1	Timer/Counter 1 (16-bit)
	0x4006_0000	TC0	Timer/Counter 0 (16-bit)
GPIO	0x4005_8000	IOCONF	IO Configuration
	0x4005_5000	GPIO5	General Purpose IO Group 5
	0x4005_4000	GPIO4	General Purpose IO Group 4
	0x4005_3000	GPIO3	General Purpose IO Group 3
	0x4005_2000	GPIO2	General Purpose IO Group 2
	0x4005_1000	GPIO1	General Purpose IO Group 1
	0x4005_0000	GPIO0	General Purpose IO Group 0
ADC	0x4004_0000	ADC	Analog to Digital Converter
FRT	0x4003_1000	FRT	Free Running Timer (32-bit)
WDT	0x4003_0000	WDT	WatchDog Timer
SYSTEM	0x4002_0000	CM	Clock Manager

	Base Address	Peripheral	Description
MEMORY	0x4001_0000	PFC	(Program) Flash Controller
SFM	0x4000_0000	-	Device information including Chip ID

4 ELECTRICAL DATA

4.1 ABSOLUTE MAXIMUM RATINGS

Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. The functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 4-1 Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating	Unit
DC supply voltage for VDD core	V_{DD_CORE}	-	–0.3 to 6.0	V
DC supply voltage for I/O	V_{DD_IO}	-	–0.3 to 6.0	V
DC supply voltage for AVref	AV_{REF}	-	–0.3 to 6.0	V
Digital I/O input voltage	V_{IN}	-	–0.3 to V_{DD_IO} + 0.3	V
Analog I/O input voltage	AV_{IN}	-	–0.3 to AV_{REF} + 0.3	V
DC digital input current	I_{IN_D}	All Input Pins	-	mA
		Per Pin	-	mA
DC analog input current	I_{IN_A}	All Input Pins	-	mA
		Per Pin	-	mA
Output current low	I_{O_LOW}	All Output Pins	-	mA
		Per Pin	-	mA
Output current high	I_{O_HIGH}	All Output Pins	-	mA
		Per Pin	-	mA
Output voltage	V_O	All Output Pins	–0.3 to V_{DD_IO} + 0.3	V
Latch up current	I_{LATCH}	-	±100	mA
Operating temperature	T_A	-	–40 to 85	°C
Storage temperature	T_{STG}	-	–65 to 155	°C

NOTE: The device is not guaranteed to operate properly above those listed in ‘Absolute Maximum Ratings’.

4.2 RECOMMENDED OPERATING CONDITIONS

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges. Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

Table 4-2 Recommended Operating Conditions

Parameter	Symbol	Conditions	Rating	Unit
DC supply voltage for V_{DD} core	V_{DD_CORE}	-	1.8 to 5.5	V
DC supply voltage for I/O	V_{DD_IO}	-	1.8 to 5.5	V
DC supply voltage for V_{LCD}	V_{LCD}	-	1.8 to 5.5	V
DC supply voltage for AV_{REF}	AV_{REF}	-	1.8 to 5.5	V
Operating temperature	T_A	-	–40 to 85	°C

4.3 D.C. ELECTRICAL CHARACTERISTICS

4.3.1 I/O CHARACTERISTICS

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
-	V_{DD}	-	1.8	-	5.5	V
Input high voltage	V_{IH1}	nRESET	0.85 V_{DD}	-	-	V
	V_{IH2}	All input pins except V_{IH1} and V_{IH3}	0.8 V_{DD}	-	-	V
	V_{IH3}	SCL0/1, SDA0/1, USARTRXD0/1/2	0.7 V_{DD}	-	-	V
	V_{IH4}	XIN, TEST	V_{DD} - 0.3 /0.7 V_{DD}	-	-	V
	V_{IH5}	XTIN	-	-	1.8V	V
Input low voltage	V_{IL1}	nRESET	-	-	0.2 V_{DD}	V
	V_{IL2}	All input pins except V_{IL1} and V_{IL3}	-	-	0.2 V_{DD}	V
	V_{IL3}	SCL0/1, SDA0/1, USARTRXD0/1/2	-	-	0.3 V_{DD}	V
	V_{IL4}	XIN, TEST	-	-	0.3/ 0.3 V_{DD}	V
	V_{IL5}	XTIN	0	-	-	V
Schmitt trigger hysteresis	V_{hys}	All input pins	0.15 V_{DD}	-	-	V
Output high voltage	V_{OH1}	I_{OH} = –1.6mA, V_{DD} = 3.0V LCD pins	V_{DD} - 0.4	-	-	V
	V_{OH2}	I_{OL} = 10mA, V_{DD} = 5.0V All output pins except V_{OH1}	V_{DD} - 1.0	-	-	V
Output low voltage	V_{OL1}	I_{OL} = 1.6mA , V_{DD} = 3.0V LCD pins	-	-	0.4	V
	V_{OL2}	I_{OL} = 10mA, V_{DD} = 5.0V All output pins except V_{OL1}	-	-	1.0	V
Input high leakage current	I_{LIH}	All input pins except XIN, XTIN, V_{IN} = V_{DD}	-	-	1	uA
	I_{LIH_XIN}	XIN, V_{IN} = V_{DD}	-	-	2	uA
Input low leakage current	I_{LIL}	All input pins except XIN, XTIN, V_{IN} = 0	-	-	– 1	uA
	I_{LIL_XIN}	XIN, V_{IN} = 0	-	-	– 2	uA
Output high leakage current	I_{LOH}	-	-	-	1	uA
Output low leakage current	I_{LOL}	-	-	-	–1	uA

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
I/O Pull-up resistor	R_{PU}	All pull-up controllable GPIO Port, V_{DD} = 5V and V_{IN} = 0 V	10	30	100	kΩ
nRESET Pull-up resistor	R_{NRST}	nRESET, V_{DD} = 5V and V_{IN} = 0 V	100	200	300	kΩ
Feedback resistor	R_{FD}	XIN Pin, V_{IN} = V_{DD} and V_{DD} = 5V	500	1000	1500	kΩ

NOTE: All pins are schmitt-trigger type.

4.3.2 I/O AC CHARACTERISTICS

Pad Type	Symbol	Frequency	Out Delay	Rising	Falling	Voltage	Load	Current
Normal	I DRV_SH	Max 20MHz		xxns	xxns	1.8 ~ 5.5V		mA

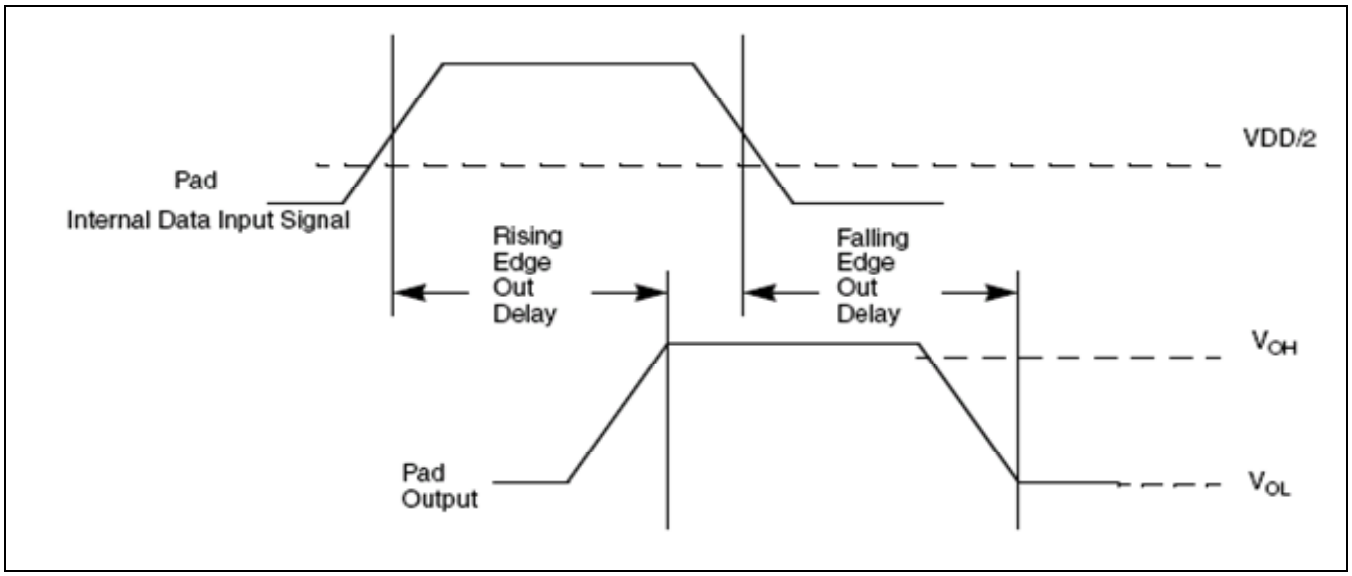

Figure 4-1 Pad Output Delay

4.3.3 I/O CAPACITANCE

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
I/O capacitance	C_{IO}	f = 1MHz, V_{DD} = 0V, unmeasured pins are connected to V_{SS}	-	-	20	pF
Input capacitance	C_{IN}		-	-		
Output capacitance	C_{OUT}		-	-		

NOTE: Not subject to production test - verified by design/characterization. Pin Px.x is connected to two pads (additionally the high-speed clock pad), so it sees twice the normal capacitance.

4.3.4 RESET INPUT CHARACTERISTICS

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
nRESET input high voltage	V_{IH_NRST}	-	0.8 V_{DD}	-	-	V
nRESET input low voltage	V_{IL_NRST}	-	-	-	0.2 V_{DD}	V
Pull-up resistor	R_{NRST}	V_{DD} = 5V and V_{IN} = 0V	100	200	300	kΩ
Input low width	t_{NRST}	-	0.8	1.2	2	us
nRESET schmitt trigger hysteresis	V_{hys_NRST}	Falling and rising edge	-	250	-	mV

NOTE: If the width of interrupt or reset pulse is greater than minimum value, the pulse is always recognized as a valid pulse.

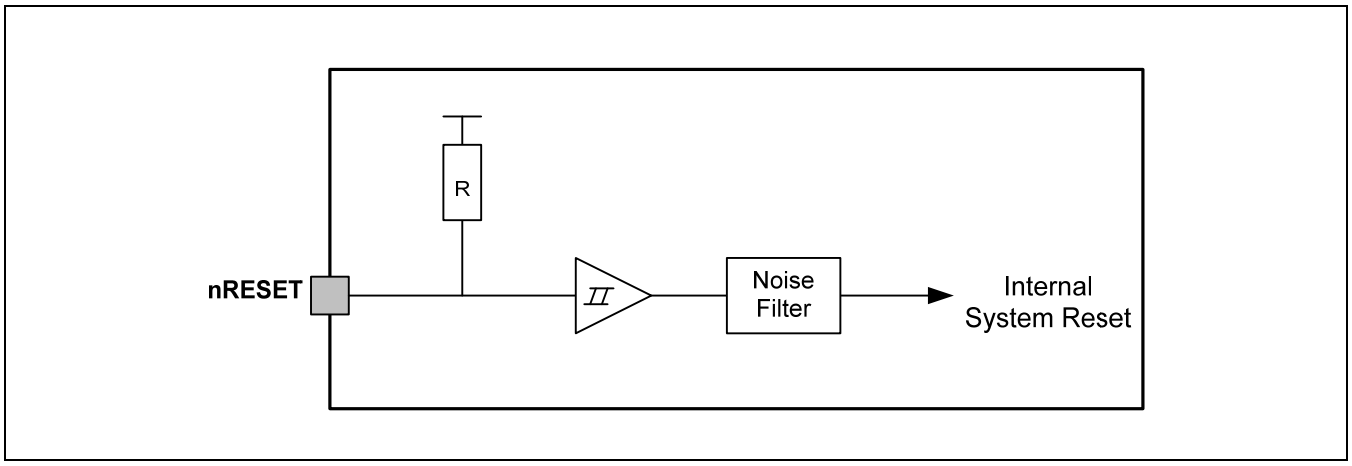

Figure 4-2 nRESET

4.3.5 EXTERNAL INTERRUPT INPUT CHARACTERISTICS

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Interrupt input high width	t_{INTH}	-	100	200	300	ns
Interrupt input low width	t_{INTL}	GPIO Port at V_{DD} = 5.0V	100	200	300	ns
Schmitt trigger with hysteresis		Falling and rising	-	250	-	mV

NOTE: You must keep a larger value than the Minimum value.
All interrupt/ wakeup inputs must have Schmitt trigger characteristics with hysteresis (falling rising edge)

4.3.6 EXTERNAL MAIN OSCILLATOR CHARACTERISTICS

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Oscillator	Symbol	Conditions	Min.	Typ.	Max.	Unit
Oscillator frequency	F_{EXTOSC}	-	1	-	20	MHz
Feedback resistor	R_{FD}	XIN Pin, V_{IN} = V_{DD} and V_{DD} = 5V	500	1000	1500	kΩ
Oscillator startup time	T_{STA}	V_{DD} is stabilized, Wakeup	-	-	5	ms
Recommended load capacitance	$C_{EXTOSC1}$, $C_{EXTOSC2}$	-	-	TBD	TBD	pF
Crystal/Resonator/Ceramic	F_{EXTOSC}	Main oscillation frequency	1	-	20	MHz
External clock	F_{EXTOSC}	XIN input frequency	1(TBD)	-	20(TBD)	MHz

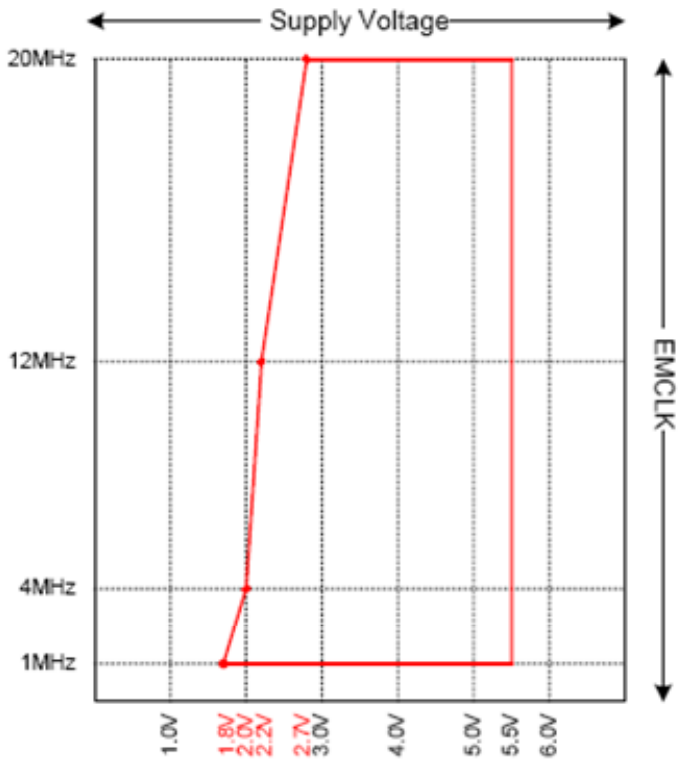

Figure 4-3 EMCLK Operating Zone by Supply Voltage

4.3.7 EXTERNAL SUB OSCILLATOR CHARACTERISTICS

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Oscillator	Symbol	Conditions	Min.	Typ.	Max.	Unit
Oscillator frequency	F_{EXTOSC}	-	-	32.768	-	kHz
Oscillator Startup Time	T_{STA}	V_{DD} is stabilized, Wakeup	-	-	10	s
Crystal/Resonator/Ceramic	F_{EXTOSC}	-	-	32.768	-	kHz
External clock	F_{EXTOSC}	The oscillation of an external clock should be 1.8v ± 10%. XTIN = 1.8V±10% external clock	TBD	-	TBD	MHz

4.3.8 INTERNAL MAIN OSCILLATOR CHARACTERISTIC

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Oscillator	Symbol	Conditions	Min.	Typ.	Max.	Unit
Internal oscillator frequency	$F_{INT1MOSC}$	Smart option IMSEL[1:0] = 11’b	-	20	-	MHz
	$F_{INT2MOSC}$	Smart option IMSEL[1:0] = 10’b	-	16	-	
	$F_{INT3MOSC}$	Smart option IMSEL[1:0] = 01’b	-	8	-	
Output clock duty ratio	T_{INTMOD}	-	40	-	60	%
Accuracy		-	-	1	6	%
Stabilization Time		Internal oscillator stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range.	-	-	10	Clk

4.3.9 INTERNAL SUB OSCILLATOR CHARACTERISTIC

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Oscillator	Symbol	Conditions	Min.	Typ.	Max.	Unit
Internal oscillator frequency	$F_{INT1MOSC}$	-	-	32.768	-	kHz
Output clock duty ratio	$T_{INT1MOD}$	-	40	-	60	%
Accuracy			-	-	50	%
Stabilization Time		Internal oscillator stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range.	-	-	10	clk

4.3.10 OSCILLATOR STABILIZATION TIME

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Stabilization Time for xxCLK	Test Condition	Min.	Typ.	Max.	Unit
IVC	Internal Voltage Converter Time when IVC Voltage is equal to 1.2V	-	-	100	us
External main clock 1~20MHz oscillator (EMCLK)	Oscillation stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range.	-	-	5	ms
External Sub-Clock 32.768kHz oscillator (ESCLK)	Oscillation stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range.	-	-	10	s
Internal main clock 20MHz oscillator (IMCLK)	Internal oscillator stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range.	-	-	10	clk
Internal Sub-Clock 32.768kHz oscillator (ISCLK)	Internal oscillator stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range.	-	-	10	clk
PLL stabilization time (PLLCLK)	PLL stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range.	-	-	200	Us
USBPLL stabilization time (USBPLLCLK)	PLL stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range.	-	-	200	Us

NOTE: All timing requirements apply to worst case conditions with respect to * full temperature range, * full microcontroller supply voltage range. (RFQ)

4.3.11 CURRENT CONSUMPTION

4.3.11.1 V_{DD} = 5.5V, USB OFF

(T_A = –40 to 85°C, V_{DD} = 5.5V)

Parameter	Symbol	Condition	Mode	Min.	Typ.	Max.	Unit
Supply current	I_{DD11}	Enable EMCLK, IMCLK, ESCLK, and ISCLK Enable all peripherals Run CPU by EMCLK	Normal operating 1	-	15	TBD	mA
	I_{DD12}	Disable EMCLK Enable IMCLK, ESCLK, and ISCLK Enable all peripherals Run CPU by IMCLK	Normal operating 2	-	13	TBD	mA
	I_{DD2}	Enable PLL Enable EMCLK, IMCLK, ESCLK, and ISCLK Run CPU by PLLCLK	High-speed operating	-	25	TBD	mA
	I_{DD31}	CPU stops in I_{DD11} Condition.	Normal idle 1	-	3.5	TBD	mA
	I_{DD32}	CPU stops in I_{DD12} Condition.	Normal idle 2	-	2.5	TBD	mA
	I_{DD4}	CPU stops in I_{DD2} Condition.	High-speed idle	-	6	TBD	mA
	I_{DD51}	Disable EMCLK, and IMCLK Enable ESCLK, and ISCLK Enable all peripherals Run CPU by ESCLK	Sub-operating 1	-	20	TBD	uA
	I_{DD61}	CPU stops in I_{DD51} Condition. LVD OFF, LCD OFF	Sub-idle 1	-	3	TBD	uA
	I_{DD62}	CPU stops in I_{DD52} Condition. LVD OFF, LCD OFF	Sub-idle 2	-	1.2	TBD	uA
	I_{DD71}	Disable EMCLK, IMCLK, ESCLK, and ISCLK All peripherals stop.	Stop 1	-	0.5	TBD	uA
	I_{DD72}	Disable EMCLK, IMCLK, and ESCLK Enable ISCLK, FRT LVD OFF, LCD OFF	Stop 2	-	1.0	TBD	uA

4.3.11.2 V_{DD} = 3.6V, USB OFF

(T_A = –40 to 85°C, V_{DD} = 3.6V)

Parameter	Symbol	Condition	Mode	Min.	Typ.	Max.	Unit
Supply current	I_{DD11}	Enable EMCLK, IMCLK, ESCLK, and ISCLK Enable all peripherals Run CPU by EMCLK	Normal operating 1	-	7.5	TBD	mA
	I_{DD12}	Disable EMCLK Enable IMCLK, ESCLK, and ISCLK Enable all peripherals Run CPU by IMCLK	Normal operating 2	-	6.5	TBD	mA
	I_{DD2}	Enable PLL Enable EMCLK, IMCLK, ESCLK, and ISCLK Run CPU by PLLCLK	High-speed operating	-	12.5	TBD	mA
	I_{DD31}	CPU stops in I_{DD11} Condition.	Normal idle 1	-	2	TBD	mA
	I_{DD32}	CPU stops in I_{DD12} Condition.	Normal idle 2	-	1.5	TBD	mA
	I_{DD4}	CPU stops in I_{DD2} Condition.	High-speed idle	-	3	TBD	mA
	I_{DD51}	Disable EMCLK, and IMCLK Enable ESCLK, and ISCLK Enable all peripherals Run CPU by ESCLK	Sub-operating 1	-	13	TBD	uA
	I_{DD61}	CPU stops in I_{DD51} Condition. LVD OFF, LCD ON	Sub-idle 1	-	3	TBD	uA
	I_{DD62}	CPU stops in I_{DD51} Condition. LVD OFF, LCD OFF	Sub-idle 2	-	1.2	TBD	uA
	I_{DD71}	Disable EMCLK, IMCLK, ESCLK, and ISCLK All peripherals stop.	Stop 1	-	0.5	TBD	uA
	I_{DD72}	Disable EMCLK, IMCLK, and ESCLK Enable ISCLK, FRT LVD OFF, LCD OFF	Stop 2	-	1	TBD	uA

4.3.11.3 V_{DD} = 1.8V, USB OFF

(T_A = –40 to 85°C, V_{DD} = 1.8V)

Parameter	Symbol	Condition	Mode	Min.	Typ.	Max.	Unit
Supply current	I_{DD11}	Enable EMCLK, IMCLK, ESCLK, and ISCLK Enable all peripherals Run CPU by EMCLK	Normal operating 1	-	TBD	TBD	mA
	I_{DD12}	Disable EMCLK Enable IMCLK, ESCLK, and ISCLK Enable all peripherals Run CPU by IMCLK	Normal operating 2	-	TBD	TBD	mA
	I_{DD2}	Enable PLL Enable EMCLK, IMCLK, ESCLK, and ISCLK Run CPU by PLLCLK	High-speed operating	-	TBD	TBD	mA
	I_{DD31}	CPU stops in I_{DD11} Condition.	Normal idle 1	-	TBD	TBD	mA
	I_{DD32}	CPU stops in I_{DD12} Condition.	Normal idle 2	-	TBD	TBD	mA
	I_{DD4}	CPU stops in I_{DD2} Condition.	High-speed idle	-	TBD	TBD	mA
	I_{DD51}	Disable EMCLK, and IMCLK Enable ESCLK, and ISCLK Enable all peripherals Run CPU by ESCLK	Sub-operating 1	-	TBD	TBD	uA
	I_{DD52}	Disable EMCLK, IMCLK, and ESCLK Enable ISCLK Enable all peripherals Run CPU by ISCLK	Sub-operating 2	-	TBD	TBD	uA
	I_{DD61}	CPU stops in I_{DD51} Condition. LVD OFF, LCD OFF	Sub-idle 1	-	TBD	TBD	uA
	I_{DD62}	CPU stops in I_{DD52} Condition. LVD OFF, LCD OFF	Sub-idle 2	-	TBD	TBD	uA
	I_{DD71}	Disable EMCLK, IMCLK, ESCLK, and ISCLK All peripherals stop.	Stop 1	-	TBD	TBD	uA
	I_{DD72}	Disable EMCLK, IMCLK, and ESCLK Enable ISCLK, FRT LVD OFF, LCD OFF	Stop 2	-	TBD	TBD	uA

NOTE: Above tables, the current is based on LVD-OFF condition.
To know the current value with LVD-ON, user should add I_{LVD} from the following current table.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
EMOSC current	I_{EMOSC}	-	-	TBD	TBD	uA
IMOSC current	I_{IMOSC}	Accuracy TBD %, Max. Operating voltage	-	TBD	TBD	uA
ESOSC current	I_{ESOSC}	Max. Operating voltage	-	TBD	TBD	uA
ISOSC current	I_{ISOSC}	Accuracy TBD %, Max. Operating voltage	-	TBD	TBD	uA
LVD current	I_{LVD}	Max. Operating voltage	-	TBD	TBD	uA
LCD current	I_{LCD}	Max. Operating voltage	-	TBD	TBD	uA
ADC current	I_{ADC}	-	-	TBD	TBD	uA
USB current	I_{USB}	-	-	TBD	TBD	uA

4.3.12 SYSTEM PLL CHARACTERISTICS

(T_A = –40 to 85 °C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input frequency	F_{IN}	-	1	-	20	MHz
Output frequency	F_{OUT}	-	12	-	40	MHz
Output clock duty ratio	T_{OD}	-	40	50	60	%
Locking time	T_{LT}	-	-	-	200	us
PLL jitter	T_J	-	-	-	TBD	ps_{p-p}

4.3.13 USB PLL CHARACTERISTICS

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input frequency	F_{IN}	-	1	-	20	MHz
Output frequency	F_{OUT}	-	-	48	-	MHz
Output clock duty ratio	T_{OD}	-	40	50	60	%
Locking time	T_{LT}	-	-	-	200	us
PLL jitter	T_J	-	-	-	TBD	ps_{p-p}

Typical values measured at AVDD18A = AVDD18D = 1.2V, AVSS18A = AVSS18D = 0V; RESETB = 1.8V; T_A = 25°C.

4.3.14 POR CHARACTERISTIC

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
POR detection voltage	-	-	-	1.2	-	V

4.3.15 IVC CHARACTERISTIC

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
IVC voltage	-	-	-	1.8	-	V

4.3.16 LVD CHARACTERISTIC

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
LVD detect voltage at V_{DD} falling	V_{LVD0}	Reset default	1.6	1.7	1.8	V
	V_{LVD1}	-	1.8	1.9	2.0	
	V_{LVD2}	-	2.0	2.1	2.2	
	V_{LVD3}	-	2.5	2.6	2.7	
	V_{LVD4}	-	2.6	2.8	3.0	
	V_{LVD5}	-	3.6	3.8	4.0	
	V_{LVD6}	-	4.1	4.3	4.5	
Hysteresis voltage of V_{LVD} (Slew Rate of LVD)	ΔV_{LVD}	-	-	100	200	mV

User can select the level for reset and interrupt voltage by LVDRL[2:0] and LVDINTL[2:0] in clock and power manager.

4.3.17 10-BIT A/D CONVERTER ELECTRICAL CHARACTERISTICS

(T_A = –40 to 85°C, VDDCORE0 = 1.8V to 5.5V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	-	-	-	10	-	Bit
ADC supply voltage	V_{ADC}	-	2.7	-	5.5	V
ADC reference voltage range	V_{AREF}	-	1.8	-	VDDCORE0	V
ADC input voltage range	V_{AIN}	-	AVSS	-	VDDCORE0	V
ADC clock frequency	f_{ADC}	50% duty cycle	-	-	2	MHz
Conversion time	t_{ADC}	FADC	20	-	-	us
Integral Non-Linearity	INL	AVREF = 5.0V, AVss = GND	-	± 1	± 2	LSB
Differential Non-Linearity	DNL	AVREF = 5.0V, AVss = GND	-	± 0.5	± 1	LSB
Top/Bottom offset Error	OE	AVREF = 5.0V, AVss = GND	-	± 1	± 3	LSB
Operating current	I	-	-	0.5	1.5	mA
Power down current	I	-	-	-	TBD	uA

4.3.18 LCD ELECTRICAL CHARACTERISTICS

(T_A = –40 to 85 °C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
LCD voltage dividing resistor	R_{LCD}	T_A = 25°C	70	110	150	kΩ
$\|V_{LCD}$ – COMi$\|$ voltage drop	V_{DC}	–15μA per common pin	-	45	120	mV
$\|V_{LCD}$ – SEGx$\|$ voltage drop	V_{DS}	–15μA per common pin	-	45	120	mV
LCD drive voltage (Capacitor Bias)	V_{LC1}	CLEVEL = 0	Typ × 0.85	TBD	Typ × 1.15	V
		CLEVEL = 1		TBD		
		CLEVEL = 2		TBD		
		CLEVEL = 3		TBD		
		CLEVEL = 4		TBD		
		CLEVEL = 5		TBD		
		CLEVEL = 6		TBD		
		CLEVEL = 7		TBD		
	V_{LC2}		$2 \times V_{LC1} \times 0.9$	TBD	$2 \times V_{LC1} \times 1.1$	
	V_{LC3}		3 × VLC1 × 0.9		3 × VLC1 × 1.1	
	V_{LC4}		4 × VLC1 × 0.9		4 × VLC1 × 1.1	
	V_{LC5}		$5 \times V_{LC1} \times 0.9$		$5 \times V_{LC1} \times 1.1$	

4.4 MEMORY CHARACTERISTICS

4.4.1 FLASH ROM ELECTRICAL CHARACTERISTICS

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Total size	Fsize	-	-	128	-	KB
Program size	Fwsize	-	-	4	-	Byte
Page size	Fpsize	-	-	512	-	Byte
Sector size	Fssize	-	-	16	-	KB
Programming time for 1word	Ftw	-	20	25	30	us
Page erase time	Ftpera	-	4	8	12	ms
Sector erase time	Ftsera	-	10	20	28	ms
Chip erase time	Ftcera	-	32	50	70	ms
Operating frequency (Data Access Time)	Ft	-	-	-	25	MHz
Endurance: Number of writing/erasing	Fnwe	-	10,000	-	-	Times
Data retention	Ftdr	-	10	-	-	Years

4.5 TIMING CHARACTERISTICS

4.5.1 I2C TIMING CHARACTERISTICS

Parameter	Symbol	Standard-Mode I2C Bus		Fast-Mode I2C Bus		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	FSCL	0	100	0	400	kHz
Bus free time between a STOP and START condition	TBUF	4.7	-	1.3	-	us
Hold time (repeated) START condition. After this period, the first clock pulse is generated	THD;STA	4.0	-	0.6	-	us
Low period of the SCL clock	TLOW	4.7	-	1.3	-	us
High period of the SCL clock	THIGH	4.0	-	0.6	-	us
Set-up time for a repeated START condition	TSU;STA	4.7	-	0.6	-	us
Data hold time	THD;DAT	0	-	0	0.9	us
Data set-up time	TSU;DAT	250	-	100	-	us
Rise time for both SDA and SCL signals	Tr	-	1000	20+01Cb	300	ns
Fall time for both SDA and SCL signals	Tf	-	300	20+01Cb	300	ns
Set-up time for STOP condition	TSU;STO	4.0	-	0.6	-	uF
Capacitive load for each bus line	Cb	-	400	-	400	uF

4.5.2 USB TIMING CHARACTERISTICS

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	USBVDD	-	3.0	3.3	3.6	V
Differential input sensitivity	VDI	-	0.2	-	-	V
Differential common mode voltage	VCM	-	0.8	-	2.5	V
Low level input voltage	USB_VIL	-		-	0.8	V
High level input voltage	USB_VIH	-	2.0	-	-	V
Low level output voltage	USB_VOL	RL = 1.5kΩ to + 3.6V		-	0.3	V
High level output voltage	USB_VOH	RL = 15kΩ to GND	2.8	-	3.6	V
Tri-state leakage current	ILZ	-	-10	-	10	uA
Transceiver capacitance	Cin	Pin to GND		-	10	pF
Pull down resistance on pins DPR/DNR	RPD	External pull down resistor	10	-	20	kΩ
Pull up resistance on DP	RPU	Enable internal resistor	1	-	2	kΩ
Driver output impedance	ZDRV	Steady-state drive (NOTE)	28	-	44	Ω
Input impedance	ZINP	-	10	-		MΩ
Termination voltage for upstream port pull up	VTERM	-	3.0	-	3.6	V

NOTE: Includes internal resistors of 30Ω 10% on both DPR and DNR.

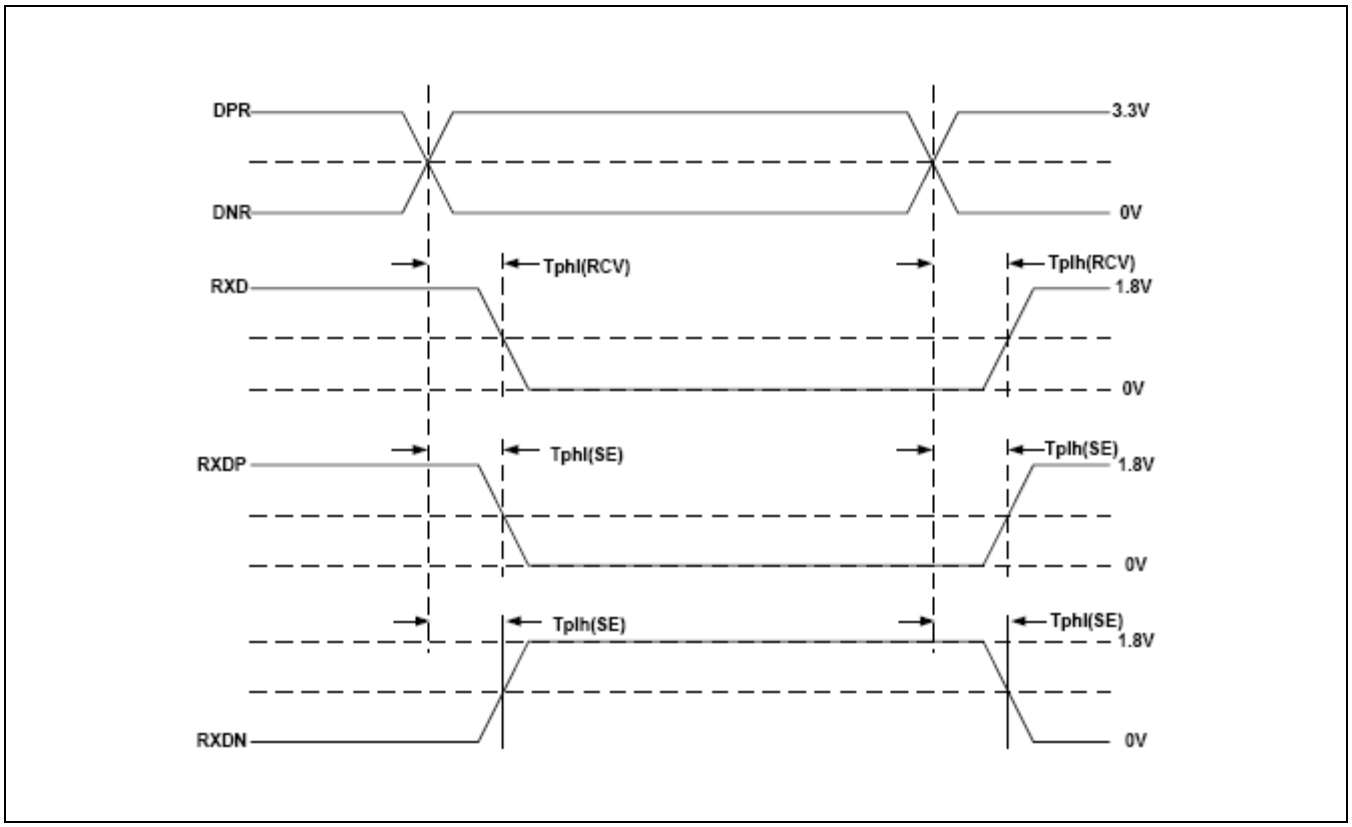

Figure 4-4 Timing Diagram of Port (pbusbfs)

NOTE: The actual port (pbusbfs) output delay values are included in the D/K DB by chracterization.

5 PACKAGE SPECIFICATION

5.1 OVERVIEW

This chapter describes the package information of S3FN21D. It is available in a 176-LQFP-2424 package type.

Table 5-1 Package Specification Information

Package Number	176 - LQFP - 2424
Package Width × Package Length	24.0 × 24.0mm
Mounting Height	1.60mm MAX
Lead Pitch	0.50mm

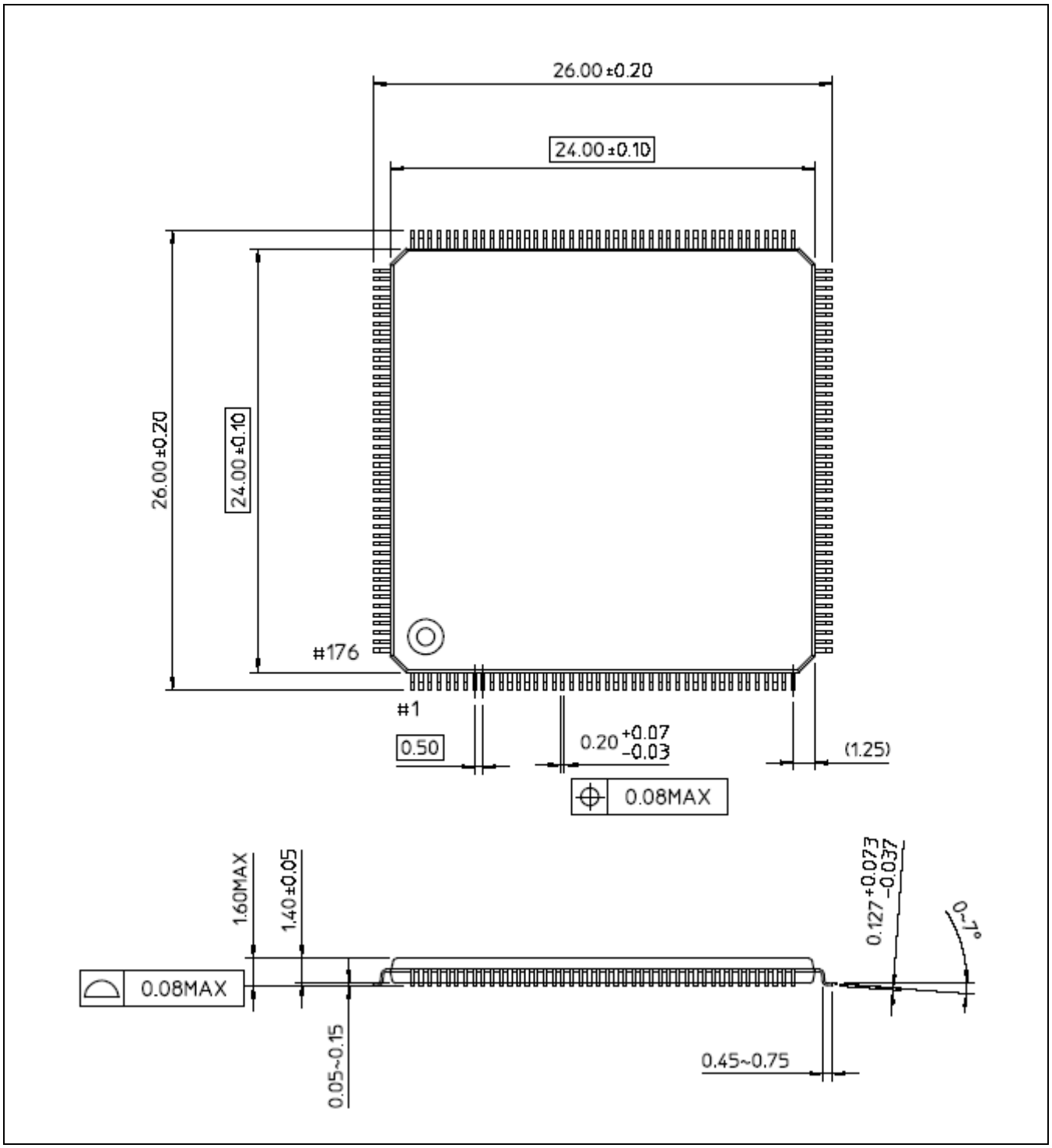

Figure 5-1 176-LQFP-2424 Package Dimension