Preliminary Datasheet

High-Performance Multimedia Processor

AMAZON-II

Hardware Manual

Advanced Digital Chips, Inc.

Rev. 1.2

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Subject to Change Without Notice.

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Revision History

Feb. 06, 2013	1st version released
Aug. 02, 2013	Updated Memory map area
Jan. 16, 2014	Corrected the error of the timer bit digits.
Jan. 22, 2014	Removed unsupported registers in the SD TV encoder section.
Sep. 15. 2014	Added DAC power down bits
Oct. 14. 2014	Corrected the pclk default value
Oct. 31. 2014	Corrected UART register address
Dec. 11. 2014	Corrected LCD clock input and Sound mixer channels
May. 14. 2015	Corrected System contorl register
May. 18. 2015	Remove EIRQ1
Feb. 25. 2016	Remove i2s channel1 IRQ enable register
Aug. 26. 2016	Corretected the address of I2S registers
Apr. 7. 2017	Corretected the address of PIN Mux module
Oct. 15. 2017	Added Reset timgin diagram
Dec. 5. 2017	Added open drain write
Dec. 12. 2017	GPIO address corrected

1 Descriptions and Features

1.1 General Description

The AMAZON-II is based on the high-performance 32-bit RISC core operating at a frequency of up to 166MHz.
The RISC core has separated bus architecture to access data and program memory (Harvard Architecture), and is implemented as 5-stage pipeline EISC architecture which provides fast instruction execution.

The process(cpu) core can use a cache and SPM memory. The program cache consists of 8K-byte memory space, and the data cache consists of 8K-byte memory space. The SPM memory consists of a 16K-byte memory space that is shared between program and data space. SPM memory can be configured as Instruction, Data, or combination of the two.
The device is an optimized host processor for application with an LCD display.
The device incorporates 2D Graphics engine, JPEG decoder and Display controller.
The 2D Graphics engine supports Bit Block Transfer(BitBLT).
The JPEG decoder is to decompress the JPEG encoded image. It performs all functions required for image decompression such as Discrete Cosine Transform(DCT), Quantization and Huffman coding.
The Display controller supports 1 overlay image window, which supports various color format, 256 level alpha blending, color key, x-y position control, and etc.
The Display controller also provides up to 24 bits of digital output to interface to RGB888 devices. The digital output is capable of CCIR.601 with separate horizontal and vertical syncs.

The video capture is capable of interfacing to common video decoders(BT.656 YCbCr 4:2:2 8-bit interface).

The HD TV Encoder and SD TV encoder interface with three analog DACs that run at up to 75MHz, providing a means for 720p YPbPr video, composite NTSC/PAL video, and/or Component video output.

The device operates with off-chip connected Quad Flash. The flash memory can be used as both a program memory and a data memory. The device can access the flash memory by configuring Quad-data bit for high speed. In addition, JTAG programming lets developers download a program with high speed.

Also, the AMAZON-II can expand SRAM, Flash memory, and SD card manually. Especially, in the case of the NAND flash memory, by adapting SLC Type as well as 24-bit ECC, developers can reduce entire system design cost.

The device provides USB 2.0 Full-Speed Device/Host, 4-channel UART, 2-channel SPI, 2-channel I2S, and TWI for communication. In the case of 8-channel DMA provides more fast communication than others.

The rich peripheral set provides the ability to control external peripheral devices and communicate with external devices. For details on each of the peripherals, see the related sections later in this document.

The AMAZON-II has a complete set of development tolls. These include C compilers to simplify programming, and a Windows™ debugger interface for visibility into source code execution.

1.2 Features

- High-performance, Low-power 32-bit EISC Microprocessor
- 32-bit EISC Architecture
  - AE32000C Empress
  - Up to 166 MHz
  - 8KB 2way Instruction Cache
  - 8KB 2way Data Cache
  - Debugger with JTAG Interface
- Embedded Memory
  - 16 KB Internal SPM

- External Memory
  - DDR2 / mDDR Memory Access
    - Up to 166 Mhz
  - Serial Flash Memory Access
    - Up to 50 Mhz
    - Support Quad, Dual, Single Data Access
  - Nor Flash Memory Access
  - Nand Flash Memory Access
    - Support Nand booting

- Peripherals
  - Video Display Controller
  - HD / SD Video Encoder
  - BT.656 Digital YcbCr 4:2:2 8-bit interface
  - JPEG Decoder
  - Graphics Engine
  - Sound Mixer
  - Channel Master/Slave I2S
  - 4 Ch. AHB DMA, 2 Ch AXI DMA
  - USB Host / Device
  - SDHC
  - 64 channel Interrupt Controller
  - 1 Channel TWI
  - 2 Ch. Master/Slave SPI with 8Bytes FIFO
  - 4 Ch. 32-bit Timer/Counter with 15-bit Pre-scaler, Capture, PWM
  - 4 Ch. UART with 16Bytes FIFO, Functionally compatible with the 16550
  - 116 Port GPIO
- Operating frequency
  - Up to 166MHz

2 Block Diagram & Pin Descriptions

2.1 Block Diagram

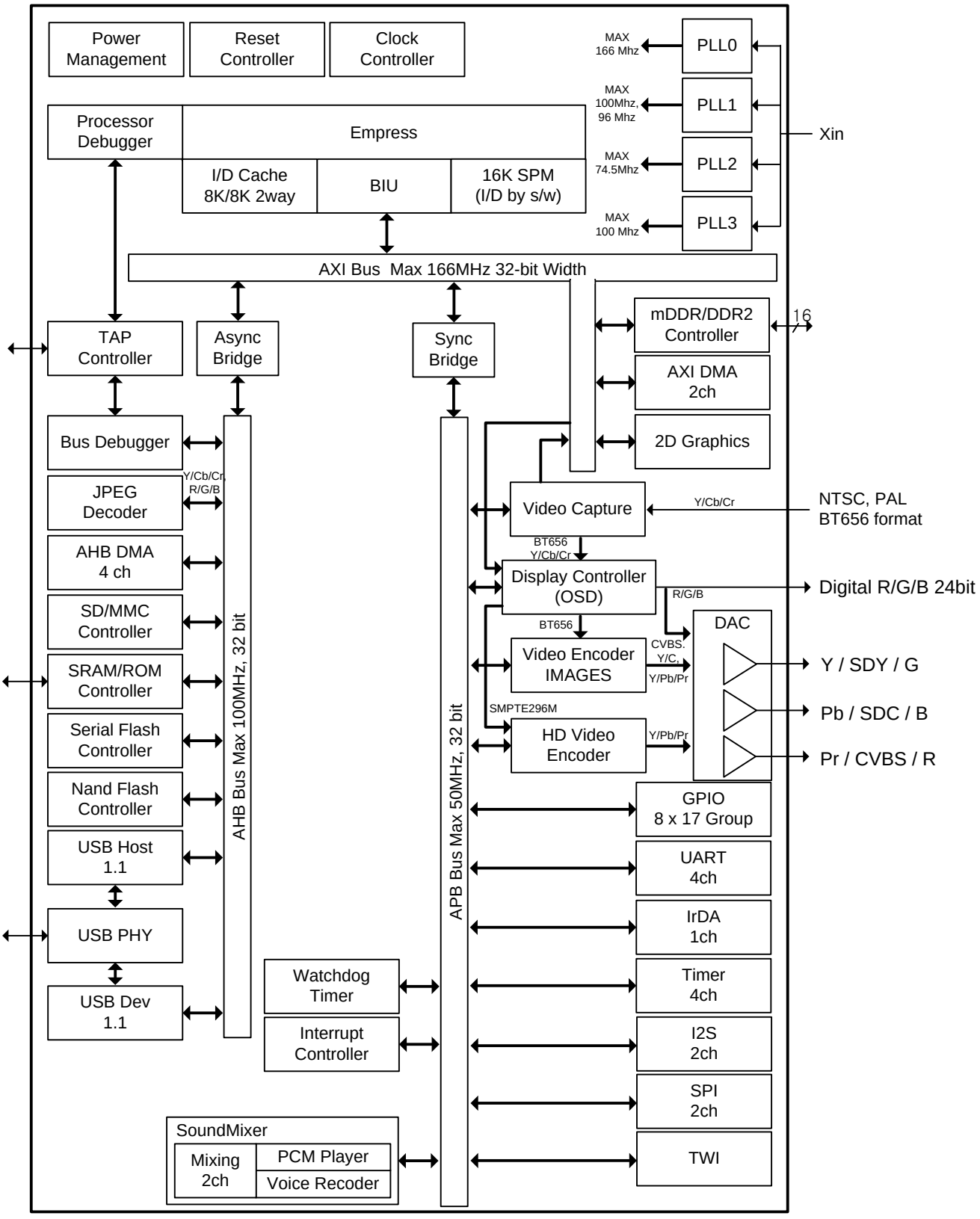


Figure 2-1 AMAZON-II Block Diagram

2.2 Pin Descriptions

2.2.1 Pin Map(Bottom View)

	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	VSS	SND_I2S_MCLK	SND_I2S_SCLK	VDD12	SND_I2S_LRCLK	LCD_D[3]	LCD_D[10]	LCD_D[15]	N.C.	LCD_D[19]	LCD_D[20]	GP14[4]	GP14[7]	OSC_DVDD33	XIN	XOUT	OSC_VSS	A
B	VDD12	GP12[2] PWMOUT1(0) SRAM_nCS[2]	LCD_DISPEN	VSS	LCD_HSYNC	LCD_D[2]	LCD_D[9]	LCD_D[14]	LCD_D[17]	LCD_D[18]	LCD_D[21]	GP14[3]	GP14[6]	PLL2_VDDA12	PLL1_VDDA12	PLL0_VDDA12	USB_DVDD33	B
C	DDR_BA[2]	GP12[3] CAPIN1(0) SRAM_nCS[3]	SND_I2S_SDO	LCD_VSYNC	SND_I2S_SDI	LCD_D[4]	LCD_D[8]	LCD_D[13]	GP13[2]	GP13[6]	LCD_D[22]	GP14[2]	GP14[5]	PLL3_VDDA12	PLL0_VSSA	nTEST	USB_DP	C
D	DDR_BA[0]	DDR_BA[1]	DDR_A[14]	LCD_D[1]	LCD_D[0]	LCD_D[23]	LCD_D[7]	LCD_D[12]	GP13[1]	GP13[5]	GP14[1]	GP0[1] NAND_D[1] UART1_RX(1)	PLL2_VSSA	PLL1_VSSA	GP0[0] NAND_D[0] UART1_TX(1)	nRESET	USB_DM	D
E	DDR_VREF1	DDR_A[13]	DDR_A[12]	DDR_A[11]	DDR_DVDD18	DDR_DVDD18	LCD_D[6]	LCD_D[11]	GP13[0]	GP13[4]	GP14[0]	GP0[2] NAND_D[2] PWMOUT1(1)	VSSA_PLL3	GP0[3] NAND_D[3] CAPIN1(1)	GP0[4] NAND_D[4] UART2_TX(1)	GP0[5] NAND_D[5] UART2_RX(1)	USB_VSS	E
F	DDR_DQS[1]	DDR_A[10]	DDR_A[9]	DDR_A[8]	DDR_DVDD18	DDR_VSS	LCD_D[5]	DVDD33	LCD_D[16]	GP13[3]	GP13[7]	GP0[6] NAND_D[6] PWMOUT2(1)	GP0[7] NAND_D[7] CAPIN2(1)	GP1[0] NAND_nCS	nTRST	TDI	TCK	F
G	VSS	DDR_A[7]	DDR_A[6]	DDR_A[5]	DDR_DVDD18	DDR_VSS	DDR_VSS	NC	DVDD33	DVDD33	GP1[1] NAND_ALE	GP1[2] NAND_CLE	GP1[3] NAND_nWE	GP1[4] NAND_nRE	GP1[5] NAND_nBUSY	TMS	TDO	G
H	DDR_nWE	DDR_A[4]	DDR_A[3]	DDR_A[2]	DDR_DVDD18	DDR_VSS	DDR_VSS	NC	VSS	VSS	GP1[6] UART_TX0	GP1[7] UART0_RX	GP2[0] SD_DAT[0] UART3_TX(1)	GP2[1] SD_DAT[1] UART3_RX(1)	GP2[2] SD_DAT[2] PWMOUT3(1)	GP2[3] SD_DAT[3] CAPIN3(1)	GP2[4] SD_CLK	H
J	DDR_nCAS	DDR_DQM[1]	DDR_A[1]	DDR_A[0]	DDR_DVDD18	NC	NC	NC	NC	NC	DVDD	GP2[5] SD_CMD	GP2[6] PWMOUT0	GP2[7] CAPIN0 SRAM_nCS1	GP3[0] I2S0_CDCLK	GP3[1] I2S0_TX_SCLK	GP3[2] I2S0_TX_WS	J
K	DDR_nRAS	DDR_D[15]	DDR_D[14]	DDR_D[13]	DDR_DVDD18	DDR_VSS	DDR_VSS	NC	VSS	VSS	DVDD33	GP3[3] I2S0_SDO	GP3[4] I2S0_SDI	GP3[5] I2S0_RX_SCLK	GP3[6] I2S0_RX_WS	GP3[7] VIN_CLK	VDD12	K
L	DDR_nCS	DDR_D[12]	DDR_D[11]	DDR_D[10]	DDR_DVDD18	DDR_VSS	DDR_VSS	NC	VSS	DVDD33	GP8[5] SRAM_A[13] I2S1_RX_SCLK(0)	GP7[6] SRAM_A[6]	GP4[0] VIN_D[0] I2S1_CDCLK(1)	GP4[1] VIN_D[1] I2S1_TX_SCLK(1)	GP4[2] VIN_D[2] I2S1_TX_WS(1)	GP4[3] VIN_D[3] I2S1_SDO(1)	VSS	L
M	VDD12	DDR_D[9]	DDR_D[8]	VSS	GP11[6] SRAM_nWAIT	GP11[4] SRAM_A[20]	GP11[2] SRAM_A[18] BOOT[2]	GP10[5] SRAM_D[13] SPI1_SCK	DVDD33	GP9[4] SRAM_D[4]	GP8[6] SRAM_A[14] I2S1_RX_WS(0)	GP7[7] SRAM_A[7]	GP7[1] SRAM_A[1]	GP4[4] VIN_D[4] I2S1_SDI(1)	GP4[5] VIN_D[5] I2S1_RX_SCLK(1)	GP4[6] VIN_D[6] I2S1_RX_WS(1)	GP4[7] VIN_D[7] EIRQ0(1)	M
N	DDR_CLKN	DDR_DQM[0]	DDR_D[7]	DVDD33	GP11[7] EIRQ0(0) LCD_PCLK	GP11[5] SRAM_A[21] LCD_VCLKIN	GP11[3] SRAM_A[19] BOOT[3]	GP10[6] SRAM_D[14] SPI1_MISO	GP10[0] SRAM_D[8] UART2_TX(0)	GP9[5] SRAM_D[5]	GP8[7] SRAM_A[15]	GP8[0] SRAM_A[8] I2S1_CDCLK(0)	GP7[2] SRAM_A[2]	GP6[5] SRAM_nRE	GP5[0] SPI0_nCS UART3_TX(0)	GP5[1] SPI0_SCK UART3_RX(0)	GP5[2] SPI0_MISO PWMOUT3(0)	N
P	DDR_CLKP	DDR_D[6]	DDR_D[5]	DDR_D[4]	GP12[0] UART1_TX(0) OHCI_PWR	DAC_RSET	DAC_VDD33	GP10[7] SRAM_D[15] SPI1_MOSI	GP10[1] SRAM_D[9] UART2_RX(0)	GP9[6] SRAM_D[6]	GP9[0] SRAM_D[0]	GP8[1] SRAM_A[9] I2S1_TX_SCLK(0)	GP7[3] SRAM_A[3]	GP6[6] SRAM_nBE1	GP5[3] SPI0_MOSI CAPIN3(0)	GP5[4] TWI_SCL	GP5[5] TWI_SDA	P
R	DDR_VREF0	DDR_D[3]	DDR_D[1]	DDR_D[0]	GP12[1] UART1_RX(0) OHCI_OVRCUR	DAC_COMP	DAC_GVDD33	GP11[0] SRAM_A[16] BOOT[0]	GP10[2] SRAM_D[10] PWMOUT2(0)	GP9[7] SRAM_D[7]	GP9[1] SRAM_D[1]	GP8[2] SRAM_A[10] I2S1_TX_WS(0)	GP7[4] SRAM_A[4]	GP6[7] SRAM_nCS0	GP5[6] SF_nCS	GP5[7] SF_CLK	GP6[0] SF_D[0]	R
T	DDR_DQS[0]	DDR_D[2]	DAC_RVSS	DDR_CKE	DAC_RVDD33	DAC_VREFIN	DAC_VSS	GP11[1] SRAM_A[17] BOOT[1]	GP10[3] SRAM_D[11] CAPIN2(0)	VSS	GP9[2] SRAM_D[2]	GP8[3] SRAM_A[11] I2S1_SDO(0)	GP7[5] SRAM_A[5]	GP7[0] SRAM_A[0]	GP6[1] SF_D[1]	VDD12	GP6[2] SF_D[2]	T
U	VSS	VDD12	DAC_IROUT	DAC_BVSS	DAC_IBOUT	DAC_BVDD33	DAC_IGOUT	DAC_GVSS	GP10[4] SRAM_D[12] SPI1_nCS	VDD12	GP9[3] SRAM_D[3]	GP8[4] SRAM_A[12] I2S1_SDI(0)	VSS	VDD12	GP6[4] SRAM_nWE	GP6[3] SF_D[3]	VSS	U
	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

2.2.2 Pin Lists

Table 2-1 AMAZON-II Pin Definitions

Signal Name	*BALL No.*	*Type*	*Function*	*Comments*
PLL0_VSSA	C3	PWR	PLL analog VDD (1.2V)	
PLL0_VDDA	B2	GND	PLL analog VSS	
PLL1_VSSA	D4	PWR	PLL analog VDD (1.2V)	
PLL1_VDDA	B3	GND	PLL analog VSS	
PLL2_VSSA	D5	PWR	PLL analog VDD (1.2V)	
PLL2_VDDA	B4	GND	PLL analog VSS	
PLL3_VSSA	E5	PWR	PLL analog VDD (1.2V)	
PLL3_VDDA	C4	GND	PLL analog VSS	
nTEST	C2	I	Test input	
nRESET	D2	I	Device reset input	
OSC_DVDD	A4	PWR	OSC supply voltage pin (3.3V)	
XIN	A3	I	Crystal oscillator input	
XOUT	A2	I/O	Crystal oscillator output	
OSC_DVSS	A1	GND	Oscillator ground	
USB_DVDD	B1	PWR	USB PHY 3.3-V supply	
USB_DP	C1	A	USB PHY data plus	
USB_DM	D1	A	USB PHY data minus	
USB_DVSS	E1	GND	USB PHY 3.3-V ground	
nTRST	F3	I	JTAG test reset	
TCK	F1	I	JTAG test clock	
TMS	G2	I	JTAG test mode select	
TDI	F2	I	JTAG test data input	
TDO	G1	O	JTAG test data output	8mA
GP0[0] NAND_D[0] UART1_TX(1)	D3	I/O	General-Purpose Input/Output(I/O) 0 pin 0. NAND Data bus[0] UART1 Transmit data output	8mA
GP0[1] NAND_D[1] UART1_RX(1)	D6	I/O	General-Purpose Input/Output(I/O) 0 pin 1. NAND Data bus[1] UART1 Receive data input	8mA
GP0[2] NAND_D[2] PWMOUT1(1)	E6	I/O	General-Purpose Input/Output(I/O) 0 pin 2. NAND Data bus[2] Timer1 PWM output	8mA
GP0[3] NAND_D[3] CAPIN1(1)	E4	I/O	General-Purpose Input/Output(I/O) 0 pin 3. NAND Data bus[3] Timer1 Capture event input	8mA
GP0[4] NAND_D[4] UART2_TX(1)	E3	I/O	General-Purpose Input/Output(I/O) 0 pin 4. NAND Data bus[4] UART2 Transmit data output	8mA
VDD	K1	PWR	1.2V core supply voltage pin	
VSS	L1	GND	Ground pin	
GP0[5] NAND_D[5] UART2_RX(1)	E2	I/O	General-Purpose Input/Output(I/O) 0 pin 5. NAND Data bus[5] UART2 Receive data input	8mA
GP0[6] NAND_D[6] PWMOUT2(1)	F6	I/O	General-Purpose Input/Output(I/O) 0 pin 6. NAND Data bus[6] Timer2 PWM output	8mA
GP0[7] NAND_D[7] CAPIN2(1)	F5	I/O	General-Purpose Input/Output(I/O) 0 pin 7. NAND Data bus[7] Timer2 Capture event input	8mA
GP1[0] NAND_nCS	F4	I/O	General-Purpose Input/Output(I/O) 1 pin 0. NAND Chip select	8mA

GP1[1] NAND_ALE	G7	I/O	General-Purpose Input/Output(I/O) 1 pin 1. NAND Address latch enable output	8mA
GP1[2] NAND_CLE	G6	I/O	General-Purpose Input/Output(I/O) 1 pin 2. NAND Command latch enable output	8mA
GP1[3] NAND_nWE	G5	I/O	General-Purpose Input/Output(I/O) 1 pin 3. NAND Write enable output	8mA
GP1[4] NAND_nRE	G4	I/O	General-Purpose Input/Output(I/O) 1 pin 4. NAND Read enable output	8mA
GP1[5] NAND_nBUSY	G3	I/O	General-Purpose Input/Output(I/O) 1 pin 5. NAND Busy input	8mA
GP1[6] UART0_TX	H7	I/O	General-Purpose Input/Output(I/O) 1 pin 6. UART0 Transmit data output	8mA
GP1[7] UART0_RX	H6	I/O	General-Purpose Input/Output(I/O) 1 pin 7. UART0 Receive data input.	8mA
DVDD	J7	PWR	3.3V I/O supply voltage pin	
DVSS	K8	GND	Ground pin	
GP2[0] SD_DAT[0] UART3_TX(1)	H5	I/O	General-Purpose Input/Output(I/O) 2 pin 0. SD Data1 I/O. Functions as data bit 0 for 4-bit SD mode and as single data bit for 1-bit SD mode UART3 Transmit data output. Functions as IrDA transmit output in IrDA mode	8mA
GP2[1] SD_DAT[1] UART3_RX(1)	H4	I/O	General-Purpose Input/Output(I/O) 2 pin 1. SD Data1 I/O. Functions as data bit 1 for 4-bit SD mode and as an IRQ input for 1-bit SD mode UART3 Receive data input. Functions as IrDA receive input in IrDA mode	8mA
GP2[2] SD_DAT[2] PWMOUT3(1)	H3	I/O	General-Purpose Input/Output(I/O) 2 pin 2. SD Data2 I/O. Functions as data bit 2 for 4-bit SD mode and as a Read Wait input for 1-bit SD mode. Timer3 PWM output	8mA
GP2[3] SD_DAT[3] CAPIN3(1)	H2	I/O	General-Purpose Input/Output(I/O) 2 pin 3. SD Data3 I/O. Functions as data bit 3 for 4-bit SD mode. Timer3 Capture event input	8mA
GP2[4] SD_CLK	H1	I/O	General-Purpose Input/Output(I/O) 2 pin 4. SD Clock output	8mA
GP2[5] SD_CMD	J6	I/O	General-Purpose Input/Output(I/O) 2 pin 5. SD Command output	8mA
GP2[6] PWMOUT0	J5	I/O	General-Purpose Input/Output(I/O) 2 pin 6. Timer0 PWM output	8mA
GP2[7] CAPIN0 SRAM_nCS1	J4	I/O	General-Purpose Input/Output(I/O) 2 pin 7. Timer1 Capture event input SRAM chip select[1]	8mA
GP3[0] I2S0_CDCLK	J3	I/O	General-Purpose Input/Output(I/O) 3 pin 0. I2S0 CODEC system clock	8mA
GP3[1] I2S0_TX_SCLK	J2	I/O	General-Purpose Input/Output(I/O) 3 pin 1. I2S0 Transmit clock	8mA
GP3[2] I2S0_TX_WS	J1	I/O	General-Purpose Input/Output(I/O) 3 pin 2. I2S0 Transmit word select	8mA
DVDD	K7	PWR	3.3V I/O supply voltage pin	
DVSS	K9	GND	Ground pin	
VDD	T2	PWR	1.2V core supply voltage pin	
VSS	U1	GND	Ground pin	
GP3[3] I2S0_SDO	K6	I/O	General-Purpose Input/Output(I/O) 3 pin 3. I2S0 Transmit data	8mA

GP3[4] I2S0_SDI	K5	I/O	General-Purpose Input/Output(I/O) 3 pin 4. I2S0 Receive data	8mA
GP3[5] I2S0_RX_SCLK	K4	I/O	General-Purpose Input/Output(I/O) 3 pin 5. I2S0 Receive clock	8mA
GP3[6] I2S0_RX_WS	K3	I/O	General-Purpose Input/Output(I/O) 3 pin 6. I2S0 Receive word select	8mA
GP3[7] VIN_CLK	K2	I/O	General-Purpose Input/Output(I/O) 3 pin 7. Video Input clock input. Input clock for 8-bit video capture.	8mA
GP4[0] VIN_D[0] I2S1_CDCLK(1)	L5	I/O	General-Purpose Input/Output(I/O) 4 pin 0. Video Input data input[0] I2S1 CODEDC system clock	8mA
GP4[1] VIN_D[1] I2S1_TX_SCLK(1)	L4	I/O	General-Purpose Input/Output(I/O) 4 pin 1. Video Input data input[1] I2S1 Transmit clock	8mA
GP4[2] VIN_D[2] I2S1_TX_WS(1)	L3	I/O	General-Purpose Input/Output(I/O) 4 pin 2. Video Input data input[2] I2S1 Transmit word select	8mA
GP4[3] VIN_D[3] I2S1_SDO(1)	L2	I/O	General-Purpose Input/Output(I/O) 4 pin 3. Video Input data input[3] I2S1 Transmit data	8mA
GP4[4] VIN_D[4] I2S1_SDI(1)	M4	I/O	General-Purpose Input/Output(I/O) 4 pin 4. Video Input data input[4] I2S1 Receive data	8mA
GP4[5] VIN_D[5] I2S1_RX_SCLK(1)	M3	I/O	General-Purpose Input/Output(I/O) 4 pin 5. Video Input data input[5] I2S1 Receive clock	8mA
GP4[6] VIN_D[6] I2S1_RX_WS(1)	M2	I/O	General-Purpose Input/Output(I/O) 4 pin 6. Video Input data input[6] I2S1 Receive word select	8mA
GP4[7] VIN_D[7] EIRQ0(1)	M1	I/O	General-Purpose Input/Output(I/O) 4 pin 7. Video Input data input[7] External interrupt input0	8mA
GP5[0] SPI0_nCS UART3_TX(0)	N3	I/O	General-Purpose Input/Output(I/O) 5 pin 0. SPI0 chip select UART3 Transmit data output	8mA
GP5[1] SPI0_SCK UART3_RX(0)	N2	I/O	General-Purpose Input/Output(I/O) 5 pin 1. SPI0 clock UART3 Receive data input	8mA
GP5[2] SPI0_MISO PWMOUT3(0)	N1	I/O	General-Purpose Input/Output(I/O) 5 pin 2. SPI0 data master-input-salve-output Timer3 PWM output	8mA
GP5[3] SPI0_MOSI CAPIN3(0)	P3	I/O	General-Purpose Input/Output(I/O) 5 pin 3. SPI0 data master-output-slave-input Timer3 Capture event input	8mA
GP5[4] TWI_SCL	P2	I/O	General-Purpose Input/Output(I/O) 5 pin 4. TWI serial clock	8mA
GP5[5] TWI_SDA	P1	I/O	General-Purpose Input/Output(I/O) 5 pin 5. TWI serial data	8mA
GP5[6] SF_nCS	R3	I/O	General-Purpose Input/Output(I/O) 5 pin 6. Serial Flash chip select	8mA
GP5[7] SF_CLK	R2	I/O	General-Purpose Input/Output(I/O) 5 pin 7. Serial Flash clock	8mA
DVDD	L8	PWR	3.3V I/O supply voltage pin	
DVSS	L9	GND	Ground pin	

GP6[0] SF_D[0]	R1	I/O	General-Purpose Input/Output(I/O) 6 pin 0. Serial Flash data bus[0]	8mA
GP6[1] SF_D[1]	T3	I/O	General-Purpose Input/Output(I/O) 6 pin 1. Serial Flash data bus[1]	8mA
GP6[2] SF_D[2]	T1	I/O	General-Purpose Input/Output(I/O) 6 pin 2. Serial Flash data bus[2]	8mA
GP6[3] SF_D[3]	U2	I/O	General-Purpose Input/Output(I/O) 6 pin 3. Serial Flash data bus[3]	8mA
GP6[4] SRAM_nWE	U3	I/O	General-Purpose Input/Output(I/O) 6 pin 4. SRAM write enable	8mA
GP6[5] SRAM_nRE	N4	I/O	General-Purpose Input/Output(I/O) 6 pin 5. SRAM read enable	8mA
VDD	U4	PWR	1.2V core supply voltage pin	
VSS	U5	GND	Ground pin	
GP6[6] SRAM_nBE1	P4	I/O	General-Purpose Input/Output(I/O) 6 pin 6. SRAM write enable for SRAM_D[15:8]	8mA
GP6[7] SRAM_nCS0	R4	I/O	General-Purpose Input/Output(I/O) 6 pin 6. SRAM chips select[0]	8mA
GP7[0] SRAM_A[0]	T4	I/O	General-Purpose Input/Output(I/O) 7 pin 0. SRAM address bus[0]	8mA
GP7[1] SRAM_A[1]	M5	I/O	General-Purpose Input/Output(I/O) 7 pin 1. SRAM address bus[1]	8mA
GP7[2] SRAM_A[2]	N5	I/O	General-Purpose Input/Output(I/O) 7 pin 2. SRAM address bus[2]	8mA
GP7[3] SRAM_A[3]	P5	I/O	General-Purpose Input/Output(I/O) 7 pin 3. SRAM address bus[3]	8mA
GP7[4] SRAM_A[4]	R5	I/O	General-Purpose Input/Output(I/O) 7 pin 4. SRAM address bus[4]	8mA
GP7[5] SRAM_A[5]	T5	I/O	General-Purpose Input/Output(I/O) 7 pin 5. SRAM address bus[5]	8mA
GP7[6] SRAM_A[6]	L6	I/O	General-Purpose Input/Output(I/O) 7 pin 6. SRAM address bus[6]	8mA
GP7[7] SRAM_A[7]	M6	I/O	General-Purpose Input/Output(I/O) 7 pin 7. SRAM address bus[7]	8mA
GP8[0] SRAM_A[8] I2S1_CDCLK(0)	N6	I/O	General-Purpose Input/Output(I/O) 8 pin 0. SRAM address bus[8] I2S1 CODEC system clock	8mA
DVDD	M9	PWR	3.3V I/O supply voltage pin	
VDD	U8	PWR	1.2V core supply voltage pin	
VSS	T8	GND	Ground pin	
GP8[1] SRAM_A[9] I2S1_TX_SCLK(0)	P6	I/O	General-Purpose Input/Output(I/O) 8 pin 1. SRAM address bus[12] I2S1 Transmit clock	8mA
GP8[2] SRAM_A[10] I2S1_TX_WS(0)	R6	I/O	General-Purpose Input/Output(I/O) 8 pin 2. SRAM address bus[12] I2S1 Transmit word select	8mA
GP8[3] SRAM_A[11] I2S1_SDO(0)	T6	I/O	General-Purpose Input/Output(I/O) 8 pin 3. SRAM address bus[12] I2S1 Transmit data	8mA
GP8[4] SRAM_A[12] I2S1_SDI(0)	U6	I/O	General-Purpose Input/Output(I/O) 8 pin 4. SRAM address bus[12] I2S1 Receive data	8mA
GP8[5] SRAM_A[13] I2S1_RX_SCLK(0)	L7	I/O	General-Purpose Input/Output(I/O) 8 pin 5. SRAM address bus[12] I2S1 Receive clock	8mA

GP8[6] SRAM_A[14] I2S1_RX_WS(0)	M7	I/O	General-Purpose Input/Output(I/O) 8 pin 6. SRAM address bus[12] I2S1 Receive word select	8mA
GP8[7] SRAM_A[15]	N7	I/O	General-Purpose Input/Output(I/O) 8 pin 7. SRAM address bus[12] External interrupt input	8mA
GP9[0] SRAM_D[0]	P7	I/O	General-Purpose Input/Output(I/O) 9 pin 0. SRAM data bus[0]	8mA
GP9[1] SRAM_D[1]	R7	I/O	General-Purpose Input/Output(I/O) 9 pin 1. SRAM data bus[1]	8mA
GP9[2] SRAM_D[2]	T7	I/O	General-Purpose Input/Output(I/O) 9 pin 2. SRAM data bus[2]	8mA
GP9[3] SRAM_D[3]	U7	I/O	General-Purpose Input/Output(I/O) 9 pin 3. SRAM data bus[3]	8mA
GP9[4] SRAM_D[4]	M8	I/O	General-Purpose Input/Output(I/O) 9 pin 4. SRAM data bus[4]	8mA
GP9[5] SRAM_D[5]	N8	I/O	General-Purpose Input/Output(I/O) 9 pin 5. SRAM data bus[5]	8mA
GP9[6] SRAM_D[6]	P8	I/O	General-Purpose Input/Output(I/O) 9 pin 6. SRAM data bus[6]	8mA
GP9[7] SRAM_D[7]	R8	I/O	General-Purpose Input/Output(I/O) 9 pin 7. SRAM data bus[7]	8mA
GP10[0] SRAM_D[8] UART2_TX(0)	N9	I/O	General-Purpose Input/Output(I/O) 10 pin 0. SRAM data bus[8] UART2 Transmit data output	8mA
GP10[1] SRAM_D[9] UART2_RX(0)	P9	I/O	General-Purpose Input/Output(I/O) 10 pin 1. SRAM data bus[9] UART2 Receive data input	8mA
GP10[2] SRAM_D[10] PWMOUT2(0)	R9	I/O	General-Purpose Input/Output(I/O) 10 pin 2. SRAM data bus[10] Timer2 PWM output	8mA
GP10[3] SRAM_D[11] CAPIN2(0)	T9	I/O	General-Purpose Input/Output(I/O) 10 pin 3. SRAM data bus[11] Timer2 Capture event input	8mA
GP10[4] SRAM_D[12] SPI1_nCS	U9	I/O	General-Purpose Input/Output(I/O) 10 pin 4. SRAM data bus[12] SPI1 chip select	8mA
GP10[5] SRAM_D[13] SPI1_SCK	M10	I/O	General-Purpose Input/Output(I/O) 10 pin 5. SRAM data bus[13] SPI1 clock	8mA
GP10[6] SRAM_D[14] SPI1_MISO	N10	I/O	General-Purpose Input/Output(I/O) 10 pin 6. SRAM data bus[14] SPI1 data master-input-slave-output	8mA
GP10[7] SRAM_D[15] SPI1_MOSI	P10	I/O	General-Purpose Input/Output(I/O) 10 pin 7. SRAM data bus[15] SPI1 data master-output-slave-input	8mA
DAC_VSS33	T11	GND	Video DAC Analog Ground	
DAC_VDD33	P11	PWR	Video DAC Analog Supply	
DAC_VREFIN	T12	I/O	Video DAC Reference IN/OUT	
DAC_RSET	P12	I	Video DAC Resistor for Reference	
DAC_COMP	R12	O	Video DAC Bias Output Voltage	
DAC_GVDD33	R11	PWR	Video DAC G Supply	
DAC_GVSS33	U10	GND	Video DAC G Ground	
DAC_IGOUT	U11	O	Video DAC G Current Output (Y)	
DAC_BVDD33	U12	PWR	Video DAC B Supply	
DAC_BVSS33	U14	GND	Video DAC B Ground	

DAC_IBOUT	U13	O	Video DAC B Current Output (Pb)	
DAC_RVDD33	T13	PWR	Video DAC R Supply	
DAC_RVSS33	T15	GND	Video DAC R Ground	
DAC_IROUT	U15	O	Video DAC R Current Output (Pr/CVBS)	
DVDD	N14	PWR	3.3V I/O supply voltage pin	
DVSS	M14	GND	Ground pin	
GP11[0] SRAM_A[16] BTMODE[0]	R10	I/O	General-Purpose Input/Output(I/O) 11 pin 0. SRAM address bus[16] Boot mode selection[0]	8mA
GP11[1] SRAM_A[17] BTMODE[1]	T10	I/O	General-Purpose Input/Output(I/O) 11 pin 1. SRAM address bus[17] Boot mode selection[1]	8mA
GP11[2] SRAM_A[18] BTMODE[2]	M11	I/O	General-Purpose Input/Output(I/O) 11 pin 2. SRAM address bus[18] Boot mode selection[2]	8mA
GP11[3] SRAM_A[19] BTMODE[3]	N11	I/O	General-Purpose Input/Output(I/O) 11 pin 3. SRAM address bus[19] Boot mode selection[3]	8mA
GP11[4] SRAM_A[20] BTMODE[4]	M12	I/O	General-Purpose Input/Output(I/O) 11 pin 4. SRAM address bus[20] Boot mode selection[4]	8mA
GP11[5] SRAM_A[21] LCD_VCLKIN	N12	I/O	General-Purpose Input/Output(I/O) 11 pin 5. SRAM address bus[21] LCD video clock input	8mA
GP11[6] SRAM_nWAIT	M13	I/O	General-Purpose Input/Output(I/O) 11 pin 6. SRAM wait input External interrupt input1	8mA
GP11[7] EIRQ0(0) LCD_PCLK	N13	I/O	General-Purpose Input/Output(I/O) 11 pin 7. External interrupt input0 LCD pixel clock output for RGB interface	8mA
VDD	U16		1.2V core supply voltage pin	
VSS	U17		Ground pin	
GP12[0] UART1_TX(0) USB_POW	P13	I/O	General-Purpose Input/Output(I/O) 12 pin 0. UART1 Transmit data output USB port power enable output (Active High)	8mA
GP12[1] UART1_RX(0) USB_OVRCUR	R13	I/O	General-Purpose Input/Output(I/O) 12 pin 1. UART1 Receive data input USB port overcurrent state input(1: Over current occurred)	8mA
DDR_DVSS18	L12	GND	DDR I/O ground pin	
DDR_D[0]	R14	I/O	DDR2 SDRAM data bus[0]	
DDR_D[1]	R15	I/O	DDR2 SDRAM data bus[0]	
DDR_DVDD18	L13	PWR	DDR I/O power supply pin	
DDR_D[2]	T16	I/O	DDR2 SDRAM data bus[2]	
DDR_D[3]	R16	I/O	DDR2 SDRAM data bus[3]	
DDR_DVSS18	L11	GND	DDR I/O ground pin	
DDR_D[4]	P14	I/O	DDR2 SDRAM data bus[4]	
DDR_D[5]	P15	I/O	DDR2 SDRAM data bus[5]	
DDR_DVDD18	K13	PWR	DDR I/O power supply pin	
DDR_D[6]	P16	I/O	DDR2 SDRAM data bus[6]	
DDR_D[7]	N15	I/O	DDR2 SDRAM data bus[7]	
DDR_DVSS18	K11	GND	DDR I/O ground pin	
DDR_DQM[0]	N16	O	DDR2 data mask output : For DDR_D[7:0]	
DDR_DQS[0]	T17	O	DDR2 data strobe inputs/outputs	
DDR_DVDD18	J13	PWR	DDR I/O power supply pin	
DDR_D[8]	M15	I/O	DDR2 SDRAM data bus[8]	

DDR_D[9]	M16	I/O	DDR2 SDRAM data bus[9]	
DDR_DVSS18	K12	GND	DDR I/O ground pin	
DDR_D[10]	L14	I/O	DDR2 SDRAM data bus[10]	
DDR_D[11]	L15	I/O	DDR2 SDRAM data bus[11]	
DDR_DVDD18	H13	PWR	DDR I/O power supply pin	
DDR_D[12]	L16	I/O	DDR2 SDRAM data bus[12]	
DDR_D[13]	K14	I/O	DDR2 SDRAM data bus[13]	
DDR_DVSS18	H12	GND	DDR I/O ground pin	
DDR_VREF[0]	R17	I	DDR voltage input for the DDR2/mDDR I/O buffers. Note even in the case of mDDR an external resistor divider connected to this pin is necessary.	
VDD	M17	PWR	1.2V core supply voltage pin	
VSS	G17	GND	Ground pin	
DDR_D[14]	K15	I/O	DDR2 SDRAM data bus[14]	
DDR_D[15]	K16	I/O	DDR2 SDRAM data bus[15]	
DDR_DVDD18	G13	PWR	DDR I/O power supply pin	
DDR_DQM[1]	J16	O	DDR2 data mask output : For DDR_D[15:8]	
DDR_DQS[1]	F17	O	DDR2 data strobe inputs/outputs	
DDR_DVSS18	H11	GND	DDR I/O ground pin	
DDR_CLKP	P17	O	DDR2 clock (positive)	
DDR_CLKN	N17	O	DDR2 clock (negative)	
DDR_CKE	T14	O	DDR2 clock enable	
DDR_DVDD18	F13	PWR	DDR I/O power supply pin	
DDR_nCS	L17	O	DDR2 chip select	
DDR_nRAS	K17	O	DDR2 row address strobe	
DDR_nCAS	J17	O	DDR2 column address strobe	
DDR_nWE	H17	O	DDR2 write enable	
DDR_DVSS18	G12	GND	DDR I/O ground pin	
DDR_A[0]	J14	O	DDR2 row/column address	
DDR_A[1]	J15	O	DDR2 row/column address	
DDR_A[2]	H14	O	DDR2 row/column address	
DDR_A[3]	H15	O	DDR2 row/column address	
DDR_A[4]	H16	O	DDR2 row/column address	
DDR_DVDD18	E13	PWR	DDR I/O power supply pin	
DDR_A[5]	G14	O	DDR2 row/column address	
DDR_A[6]	G15	O	DDR2 row/column address	
DDR_A[7]	G16	O	DDR2 row/column address	
DDR_A[8]	F14	O	DDR2 row/column address	
DDR_A[9]	F15	O	DDR2 row/column address	
DDR_A[10]	F16	O	DDR2 row/column address	
DDR_DVSS18	F12	GND	DDR I/O ground pin	
DDR_VREF[1]	E17	I	DDR voltage input for the DDR2/mDDR I/O buffers. Note even in the case of mDDR an external resistor divider connected to this pin is necessary.	
DDR_DVDD18	E12	PWR	DDR I/O power supply pin	
DDR_A[11]	E14	O	DDR2 row/column address	
DDR_A[12]	E15	O	DDR2 row/column address	
DDR_A[13]	E16	O	DDR2 row/column address	
DDR_A[14]	D15	O	DDR2 row/column address	
DDR_DVSS18	G11	GND	DDR I/O ground pin	
DDR_BA[0]	D17	O	DDR2 SDRAM bank address	
DDR_BA[1]	D16	O	DDR2 SDRAM bank address	
DDR_BA[2]	C17	O	DDR2 SDRAM bank address	
VDD	B17	PWR	1.2V core supply voltage pin	

VSS	A17	GND	Ground pin	
GP12[2] PWMOUT1(0) SRAM_nCS2	B16	I/O	General-Purpose Input/Output(I/O) 12 pin 2. Timer1 PWM output SRAM chip select[2]	8mA
GP12[3] CAPIN1(0) SRAM_nCS3	C16	I/O	General-Purpose Input/Output(I/O) 12 pin 3. Timer1 Capture input SRAM chip select[3]	8mA
SND_I2S_MCLK	A16	O	Sound I2S CODEC system clock	8mA
SND_I2S_SCLK	A15	O	Sound I2S serial clock	8mA
SND_I2S_LRCLK	A13	O	Sound I2S channel select clock	8mA
SND_I2S_SDO	C15	O	Sound I2S serial data output	8mA
LCD_DISPEN	B15	O	LCD Data enable signal for RGB interface	8mA
LCD_VSYNC	C14	O	LCD vertical sync signal for RGB interface	8mA
LCD_HSYNC	B13	O	LCD horizontal sync signal for RGB interface	8mA
SND_I2S_SDI	C13	I	I2S serial data input	
LCD_R[0]	D13	O	LCD pixel data output for RGB interface(R[0])	8mA
LCD_R[1]	D14	O	LCD pixel data output for RGB interface(R[1])	
LCD_B[7]	D12	O	LCD pixel data output for RGB interface(B[7])	8mA
LCD_R[2]	B12	O	LCD pixel data output for RGB interface(R[2])	8mA
LCD_R[3]	A12	O	LCD pixel data output for RGB interface(R[3])	8mA
DVDD	F10	PWR	3.3V I/O supply voltage pin	
LCD_R[4]	C12	O	LCD pixel data output for RGB interface(R[4])	8mA
LCD_R[5]	F11	O	LCD pixel data output for RGB interface(R[5])	8mA
LCD_R[6]	E11	O	LCD pixel data output for RGB interface(R[6])	8mA
LCD_R[7]	D11	O	LCD pixel data output for RGB interface(R[7])	8mA
LCD_G[0]	C11	O	LCD pixel data output for RGB interface(G[0])	8mA
LCD_G[1]	B11	O	LCD pixel data output for RGB interface(G[1])	8mA
LCD_G[2]	A11	O	LCD pixel data output for RGB interface(G[2])	8mA
LCD_G[3]	E10	O	LCD pixel data output for RGB interface(G[3])	8mA
LCD_G[4]	D10	O	LCD pixel data output for RGB interface(G[4])	8mA
LCD_G[5]	C10	O	LCD pixel data output for RGB interface(G[5])	8mA
LCD_G[6]	B10	O	LCD pixel data output for RGB interface(G[6])	8mA
LCD_G[7]	A10	O	LCD pixel data output for RGB interface(G[7])	8mA
LCD_B[0]	F9	O	LCD pixel data output for RGB interface(B[0])	8mA
DVSS	H9	GND	Ground pin	
DVDD	G9	PWR	3.3V I/O supply voltage pin	
N.C.	A9	O	leave open	8mA
LCD_B[1]	B9	O	LCD pixel data output for RGB interface(B[1])	8mA
LCD_B[2]	B8	O	LCD pixel data output for RGB interface(B[2])	8mA
LCD_B[3]	A8	O	LCD pixel data output for RGB interface(B[3])	8mA
LCD_B[4]	A7	O	LCD pixel data output for RGB interface(B[4])	8mA
LCD_B[5]	B7	O	LCD pixel data output for RGB interface(B[5])	8mA
VDD	A14	PWR	1.2V core supply voltage pin	
VSS	B14	GND	Ground pin	
GP13[0]	E9	I/O	General-Purpose Input/Output(I/O) 13 pin 0.	8mA
GP13[1]	D9	I/O	General-Purpose Input/Output(I/O) 13 pin 1.	8mA
GP13[2]	C9	I/O	General-Purpose Input/Output(I/O) 13 pin 2.	8mA
GP13[3]	F8	I/O	General-Purpose Input/Output(I/O) 13 pin 3.	8mA
GP13[4]	E8	I/O	General-Purpose Input/Output(I/O) 13 pin 4.	8mA
GP13[5]	D8	I/O	General-Purpose Input/Output(I/O) 13 pin 5.	8mA
GP13[6]	C8	I/O	General-Purpose Input/Output(I/O) 13 pin 6.	8mA
GP13[7]	F7	I/O	General-Purpose Input/Output(I/O) 13 pin 7.	8mA
DVDD	G8	PWR	3.3V I/O supply voltage pin	
DVSS	H8	GND	Ground pin	
LCD_B[6]	C7	O	LCD pixel data output for RGB interface(B[6])	8mA

GP14[0]	E7	I/O	General-Purpose Input/Output(I/O) 14 pin 0.	8mA
GP14[1]	D7	I/O	General-Purpose Input/Output(I/O) 14 pin 1.	8mA
GP14[2]	C6	I/O	General-Purpose Input/Output(I/O) 14 pin 2.	8mA
GP14[3]	B6	I/O	General-Purpose Input/Output(I/O) 14 pin 3.	8mA
GP14[4]	A6	I/O	General-Purpose Input/Output(I/O) 14 pin 4.	8mA
GP14[5]	C5	I/O	General-Purpose Input/Output(I/O) 14 pin 5.	8mA
GP14[6]	B5	I/O	General-Purpose Input/Output(I/O) 14 pin 6.	8mA
GP14[7]	A5	I/O	General-Purpose Input/Output(I/O) 14 pin 7.	8mA

3 Memory Architecture and Program Download

3.1 Memory Map

The memory map for the AMAZON-II is provided in Table 3-1. Upon reset the CPU boots from address 0x0000_0000,

Table 3-1 AMAZON-II Memory Map

Address	*Block*	*Remark*
0x0000_0000 ~ 0x00FF_FFFF	Boot Memory	16 MB
0x2000_0000 ~ 0x2000_3FFF	On-chip SRAM(SPM)	16 KB
0x4000_0000 ~ 0x40FF_FFFF	Serial Flash	16 MB
0x6000_0000 ~ 0x603F_FFFF	ROM / NOR CS0#	4 MB
0x6040_0000 ~ 0x607F_FFFF	ROM / NOR CS1#	4 MB
0x6080_0000 ~ 0x60BF_FFFF	ROM / NOR CS2#	4 MB
0x60C0_0000 ~ 0x60FF_FFFF	ROM / NOR CS3#	4 MB
0xC000_0000 ~ 0xC3FF_FFFF	DDR2	128 MB
0xF000_0000 ~ 0xF001_FFFF	AHB Peripherals	See Table 3-2
0xF400_0000 ~ 0xF400_5FFF	APB Peripherals	See Table 3-2

The memory map is different with boot mode

Table 3-2 Memory Map in Serial Flash Boot

Address	*Block*	*Remark*
0x0000_0000 ~ 0x00FF_FFFF	Serial Flash	16 MB
0x2000_0000 ~ 0x2000_3FFF	On-chip SRAM(SPM)	16 KB
0x4000_0000 ~ 0x40FF_FFFF	Serial Flash	16 MB
0x6000_0000 ~ 0x603F_FFFF	ROM / NOR CS0#	4 MB
0x6040_0000 ~ 0x607F_FFFF	ROM / NOR CS1#	4 MB
0x6080_0000 ~ 0x60BF_FFFF	ROM / NOR CS2#	4 MB
0x60C0_0000 ~ 0x60FF_FFFF	ROM / NOR CS3#	4 MB
0xC000_0000 ~ 0xC3FF_FFFF	DDR2	128 MB
0xF000_0000 ~ 0xF001_FFFF	AHB Peripherals	See Table 3-2
0xF400_0000 ~ 0xF400_5FFF	APB Peripherals	See Table 3-2

Table 3-3 Memory Map in NAND Flash Boot

Address	*Block*	*Remark*
0x0000_0000 ~ 0x00FF_FFFF	On-chip SRAM(SPM)	2 KB
0x2000_0000 ~ 0x2000_3FFF	On-chip SRAM(SPM)	16 KB
0x4000_0000 ~ 0x40FF_FFFF	Serial Flash	16 MB
0x6000_0000 ~ 0x603F_FFFF	ROM / NOR CS0#	4 MB
0x6040_0000 ~ 0x607F_FFFF	ROM / NOR CS1#	4 MB
0x6080_0000 ~ 0x60BF_FFFF	ROM / NOR CS2#	4 MB
0x60C0_0000 ~ 0x60FF_FFFF	ROM / NOR CS3#	4 MB
0xC000_0000 ~ 0xC3FF_FFFF	DDR2	128 MB
0xF000_0000 ~ 0xF001_FFFF	AHB Peripherals	See Table 3-2
0xF400_0000 ~ 0xF400_5FFF	APB Peripherals	See Table 3-2

Table 3-4 Memory Map in ROM/NOR Flash Boot

Address	*Block*	*Remark*
0x0000_0000 ~ 0x00FF_FFFF	ROM / NOR	16 MB
0x2000_0000 ~ 0x2000_3FFF	On-chip SRAM(SPM)	16 KB
0x4000_0000 ~ 0x40FF_FFFF	Serial Flash	16 MB
0x6000_0000 ~ 0x603F_FFFF	ROM / NOR CS0#	4 MB
0x6040_0000 ~ 0x607F_FFFF	ROM / NOR CS1#	4 MB
0x6080_0000 ~ 0x60BF_FFFF	ROM / NOR CS2#	4 MB
0x60C0_0000 ~ 0x60FF_FFFF	ROM / NOR CS3#	4 MB
0xC000_0000 ~ 0xC3FF_FFFF	DDR2	128 MB
0xF000_0000 ~ 0xF001_FFFF	AHB Peripherals	See Table 3-2
0xF400_0000 ~ 0xF400_5FFF	APB Peripherals	See Table 3-2

3.2 Memory Map for Peripherals

The register area starting at 0xF000_0000 is individually assigned 1Kbytes. Detailed information on each area as follows.

Table 3-5 Memory Map for Peripherals

Address	*Offset*	*Block*
APB F400_0000h	0000h	PMU & System
	0400h	Pin Mux
	0800h	mDDR/DDR2
	1000h	CRTC
	2000h	Video Capture
	2400h	Video Encoder
	2800h	HD Video Encoder
	2C00h	AXI DMA
	3000h	UART
	3400h	WDT
	3800h	Timer
	4000h	TWI
	4400h	I2S
	4800h	INTC
	4C00h	SPI
	5000h	Sound Mixer
AHB F000_0000h	0000h	Serial Flash Ctrl
	0400h	SRAM/NOR Ctrl
	0800h	NAND Flash Ctrl
	0C00h	SD Host Ctrl
	1000h	USB Device
	1400h	USB Host
	1800h	AHB DMA
	1C00h	GPIO
	10000h	MJPEG

4 System Reset and Clock

4.1 Reset

Reset controller consists of External Reset, JTAG Reset, and Watchdog Reset.
The following figure 4-1 shows the entire Reset signals.

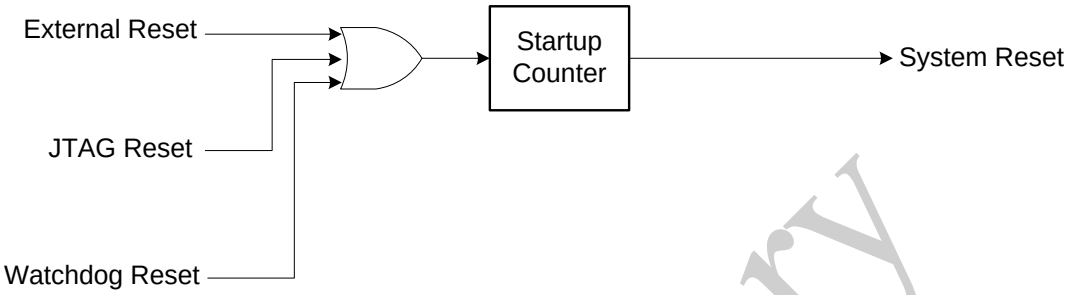


Figure 4-1 Reset

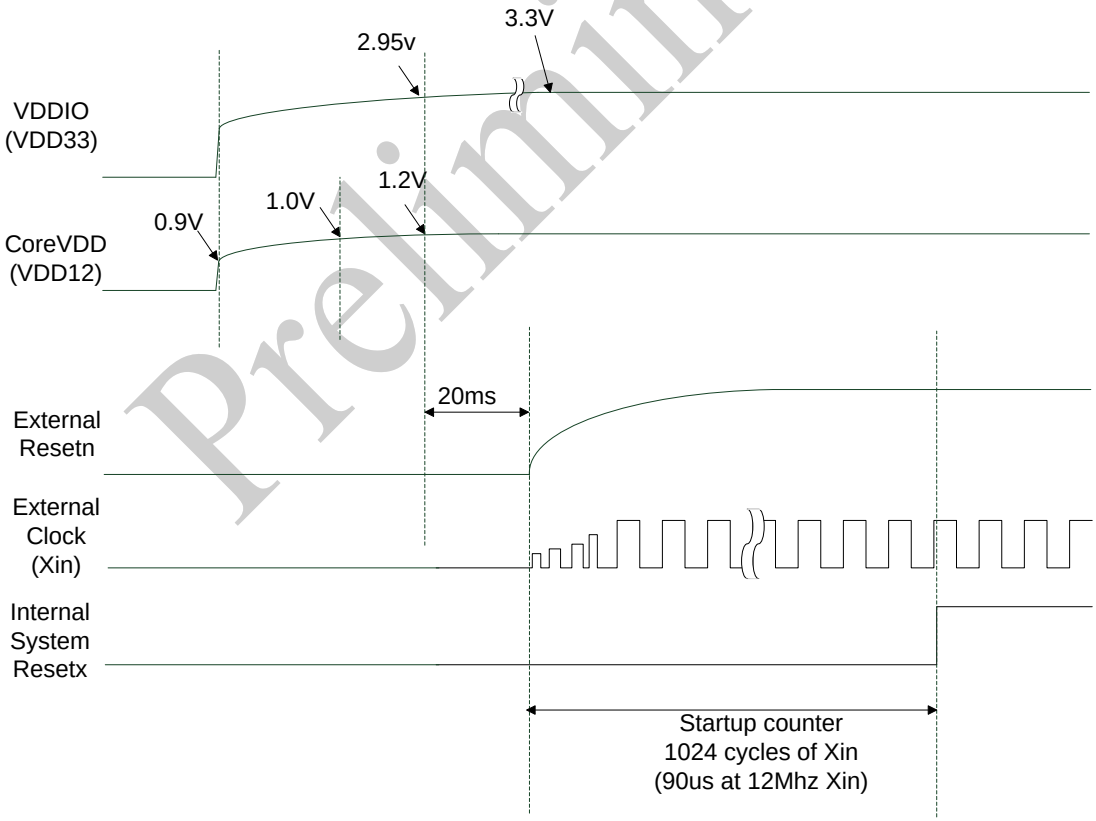


Figure 4-2 Reset Timing

4.2 Clocks

There is only one clock source for the system.

The OSC provides a frequency-accurate clock source by one of two means: an external single-ended clock source is connected to the XIN input pin, or an external crystal is connected across the XIN input and XOUT output pins. The crystal may be any one of the supported frequencies between 12 MHz and 28 MHz. The single-ended clock source range is from DC through the specified speed of the device.

The sound clock (SND_CLK) is derived from the above source plus two others: the output of the internal PLL2, and the input pin, CAPIN3 (GP2[3]/GP5[3]).

The LCD clock (DOT_CLK) is derived from the OSC, PLL3 output clock, and the input pin LCD_VCLKIN (GP11[5]).

Figure 4-2 shows the logic for the clock tree. The peripheral blocks are driven by MCLK, ACLK, PCLK and HCLK. They can be individually enabled/disabled.

The ACLK signal is a synchronous divide of the MCLK to provide the AXI peripheral blocks.

The PCLK signal is a synchronous divide of the ACLK to provide the PCLK peripheral blocks.

The HCLK signal is asynchronous to ACLK and PCLK signals.

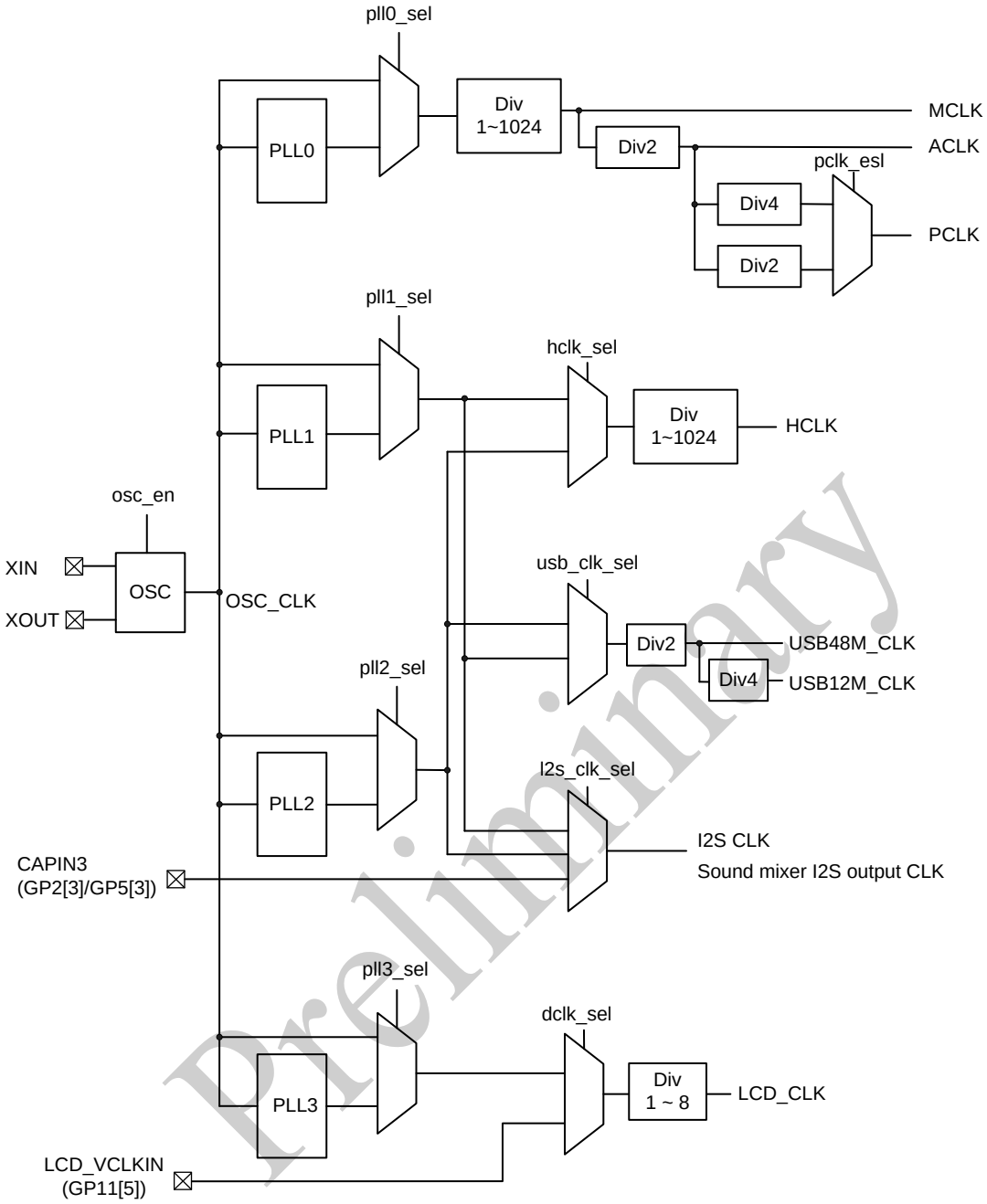


Figure 4-3 Clock Tree

4.2.1 Crystal Configuration for the Oscillator (OSC)

The oscillator supports the use of a select number of crystals. The range of supported crystals is 12 to 28 MHz.

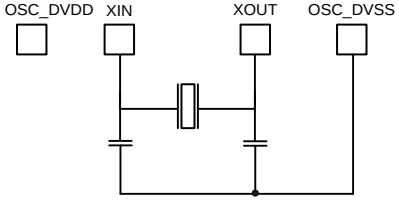


Figure 4-4 Typical Crystal Oscillator Connection

Two external capacitors must be wired as shown in Figure 4-3.

In this case, XOUT can be left unconnected.

4.2.2 PLL0/PLL1/PLL2/PLL3 Frequency Configuration

The PLLs are enabled by default during power-on reset and is disabled later by software if not required. Software specifies the output divisor to set the system clock frequency, and enables the PLLs to drive the output.

A RESET control is provided to power down the PLLs and reset it to a known state.

The PLLs has two modes of operation: Normal and Power-Down
Normal: The PLLs multiplies the input clock reference and drives the output.
Power-Down: Most of the PLLs internal circuitry is disabled and the PLLs do not drive the output.

The modes are controlled by using the RESET field in the PLL CONTROL register.

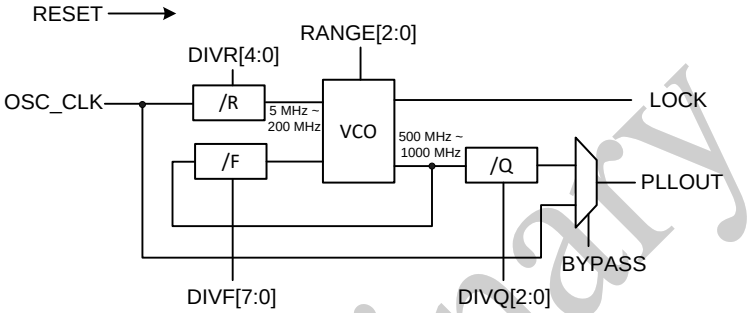


Figure 4-5 PLL Block Diagram

The PLL can accept input frequencies from 5 MHz to 200 MHz.

It has comprehensive divider options.

PLLOUT = REF * (DIVF + 1) / ((DIVR + 1) * 2 ^ DIVQ)

A LOCK signal is provided to indicate that the PLL has locked on to the incoming signal. LOCK is an asynchronous output pin, which asserts HIGH to indicate that the PLL has achieved frequency lock with a good phase lock.

The LOCK bits in System Status register reflect the LOCK signal. Software can use these fields to ensure that the PLL clock is stable.

4.3 Power Management

The AMAZON-II offers configurable and flexible power management control that allows the user to choose the best power option to fit the application.

Power management is provided via clock control to the CPU and individual peripherals.

For power-savings purposes, the Clock Enable register control the clock gating logic for each peripheral while the device is in Run, Idle, and Deep-Idle mode, respectively.

The AMAZON-II supports the following three power control modes:

- Run Mode
- Idle Mode
- Deep-Idle Mode

Run Mode

This is the default mode after any reset occurs.
To reduce power consumption, the selection of the low clock divide rate is available. It can also be programmed to stop the PLL and directly use XIN clock.

Idle Mode (Halt 3)

This mode is entered via “Halt 3” command.
In this mode, only the core clock is stopped. The peripheral clocks can be enabled. Any interrupt enables to exit Idle mode and Return to Normal Run Mode

Deep-Idle Mode (Halt 1)

This mode is entered by using “Halt 1” instruction.
In this mode all clock circuits are turned off and the main oscillator input pins are disabled. The device exits Deep Idle mode. when the external interrupt(EIRQ0) occurs.

4.4 Register Description

4.4.1 PMU Write Enable

Address : 0xF400_0000

Bit	R/W	Description	Default Value
31 : 15		Reserved	-
14		System control Register write enable	0
13		clock enable Register write enable	0
12		clock control Register write enable	0
11		PLL3 Control Register write enable	0
10		PLL2 Control Register write enable	0
9		PLL1 Control Register write enable	0
8		PLL0 Control Register write enable	0
7 :3		Reserved	-
2		Halt use enable	0
1		Software Halt Register write enable	0
0		Reserved	-

4.4.2 PLL Control Register

Address : 0xF400_0020 / 0xF400_0024 / 0xF400_0028 / 0xF400_002C

Bit	R/W	Description	Default Value
31 : 29	R	Reserved	-
28	R/W	PLL(n) reset 0 : reset 1 : No effect	1
27 : 25	R	Reserved	-
24	R/W	PLL(n) bypass 0 : normal 1 : bypass	0
23	R	Reserved	-
22 : 20	R/W	PLL(n) Filter Range This sets the PLL loop filter to work with the post-reference divider frequency. Choose the highest valid range for best jitter performance. 000 = Bypass 100 = 21 to 42 MHz 001 = 5 to 10 MHz 101 = 34 to 68 MHz 010 = 8 to 16 MHz 110 = 54 to 108 MHz 011 = 13 to 26MHz 111 = 88 to 200 MHz	000
19 : 17	R	Reserved	-
18 : 16	R/W	(DIVQ) Output Divider Value (2^Binary value, so 000 = ÷1) VCO must be within the range of 500 MHz to 1000 MHz	000
15 : 8	R/W	(DIVF) Feedback Divider Value (Binary value+1, so 00000000 = ÷1)	00000000
7 : 5	R	Reserved	-
4 : 0	R/W	(DIVR) Reference Divider Value (Binary value+1, so 00000 = ÷1) Both REF and divided REF must be within the range of 5 MHz to 200 MHz.	00000

PLLOUT = REF * (DIVF + 1) / ((DIVR + 1) * 2 ^ DIVQ)

4.4.3 Clock Control Register

Address : 0xF400_0030

Bit	R/W	Description	Default Value
20	R/W	usb clk sel 0 : PLL2 clk 1 : PLL1 clk	0
19	R	Reserved	0
18	R/W	DAC clk sel 0 : dclk 1 : ~dclk	0
17 : 16	R/W	dclk divide 00 : dclk 01 : dclk / 2 10 : dclk / 4 11 : dclk / 8	0
15 : 14	R/W	dclk sel 00 : PLL3 clk 01 : crtc clk (GP11[5]/LCD_VCLKIN) 10 : ice clk (GP3[7]/VIN_CLK)	0
13 : 12	R/W	i2s clk sel	0

		00 : PLL1 clk 01 : PLL2 clk 10 : CAPIN3 (GP2[3]/GP5[3])	
11	R/W	hclk source sel 0 : PLL1 clk 1 : PLL2 clk	0
10 : 8	R/W	hclk divide Value Divisor 0 : /1 (default) 1 : / 2 2 : / 4 3 : / 8 4 : / 16 5 : /1024	0
7	R/W	pclk sel 0 : aclk / 4 1 : aclk / 2	0
6 : 4	R/W	mclk divide select Value Divisor 0 : /1 (default) 1 : / 2 2 : / 4 3 : / 8 4 : / 16 5 : /1024	0
3	R/W	Clock source select (PLL3_SEL) Choses whether the DCLK clock is derived from the PLL3 output or the OSC source. 0 : OSC clock selected 1 : PLL3 output clock selected	0
2	R/W	Clock source select (PLL2_SEL) Choses whether the USB clock is derived from the PLL2 output or the OSC source. 0 : OSC clock selected 1 : PLL2 output clock selected	0
1	R/W	Clock source select (PLL1_SEL) Choses whether the HCLK clock is derived from the PLL1 output or the OSC source. 0 : OSC clock selected 1 : PLL1 output clock selected	0
0	R/W	Clock source select (PLL0_SEL) Choses whether the MCLK clock is derived from the PLL0 output or the OSC source. 0 : OSC clock selected 1 : PLL0 output clock selected	0

4.4.4 Clock Enable Register

Address : 0xF400_0034

Bit	*R/W*	*Description*	*Default Value*
31	R/W	Reserved	-
30	R/W	ahb bus clock enable	1
29	R/W	apb bus clock enable	1
28	R/W	axi bus clock enable	1
27 : 26	R	Reserved	-
25	R/W	usb host clock enable	1
24	R/W	usb device clock enable	1
23	R/W	mjpeg clock enable	1
22	R/W	ahb dma clock enable	1
21	R/W	sdhc clock enable	1
20	R/W	nand flash clock enable	1
19	R/W	Reserved	1
18	R/W	external sram clock enable	1
17	R/W	serial flash clock enable	1
16	R/W	gpio clock enable	1
15	R/W	Reserved	1
14	R/W	interrupt controller clock enable	1
13	R/W	i2s clock enable	1
12	R/W	spi clock enable	1
11	R/W	twi clock enable	1
10	R/W	timer clock enable	1
9	R/W	watchdog clock enable	1
8	R/W	uart clock enable	1
7	R/W	ddr clock enable	1
6	R/W	hd video encoder clock enable	1
5	R/W	video encoder clock enable	1
4	R/W	bt656 decoder clock enable	1

3	R/W	graphic engine clock enable	1
2	R/W	debugger clock enable	1
1	R/W	crtc clock enable	1
0	R/W	axi dma clock enable	1

4.4.5 System Control Register

Address : 0xF400_0038

Bit	*R/W*	*Description*	*Default Value*
31 : 12	R	Reserved	-
25 : 24	R/W	ahb irq select	0
23 : 22	R	Reserved	-
21	R/W	wake up external irq[1] mode	0
20	R/W	wake up external irq[0] mode	0
19 : 18	R	Reserved	-
17	R/W	wake up external irq[1] enable	0
16	R/W	wake up external irq[0] enable	0
15	R/W	DAC R channel power down	0
14	R/W	DAC B channel power down	0
13	R/W	DAC G channel power down	0
12	R/W	DAC power down	0
11	R/W	usb phy sel 0 : usb device 1 : usb host	0
10	R/W	Dp, Dn Logic zero output (for TEST only)	0
9	R/W	Test data input (for TEST only)	0
8	R/W	Test output enable(for TEST only)	0
7	R/W	Test select(for TEST only)	0
6	R/W	Dp , Dn pull down Enable 0 : disable 1: enable	0
5	R/W	Dn pull down Enable 0 : disable 1: enable	0
4	R/W	Dp pull down Enable 0 : disable 1: enable	0
3	R/W	Dn idle pull-up Enable 0 : enable 1: disable	0
2	R/W	Dn always pull-up Enable 0 : enable 1: disable	0
1	R/W	Dp idle pull-up Enable 0 : enable 1: disable	0
0	R/W	Dp always pull-up Enable 0 : enable 1: disable	0

4.4.1 System Status Register

Address : 0xF400_0440

Bit	*R/W*	*Description*	*Default Value*
31 : 15	R	Reserved	1
11	R	pll3 lock 0 : unlock 1 : locked	0
10	R	pll2 lock 0 : unlock 1 : locked	-
9	R	pll1 lock 0 : unlock 1 : locked	0
8	R	pll0 lock 0 : unlock 1 : locked	0
7 : 4	R	Reserved	-
3 : 1	R	Booting memory information 111 : Rom, Sram boot 110 : Serial Flash boot 101 : Nand boot MLC 24-bit 100 : Nand boot MLC 4-bit 011 : Nand boot large 5C 010 : Nand boot large 4C 001 : Nand boot small 4C 000 : Nand boot small 3C	0
0	R	Debug boot information 0 : Debug boot 1 : Normal boot	0

5 Device Configuration

This device supports a variety of boot modes. Boot mode selection is determined by the values of the BOOT pins. When device reset is released, the input states of the BOOT pins are sampled.

All boot configuration pins are multiplexed with functional pins. These pins function as boot configuration pins only during reset. The input states of these pins are sampled and latched into the SYSTEM STATUS register when reset is deasserted. After device reset is deasserted, the values on these multiplexed pins no longer have to hold the configuration.

For proper device operation, external pullup/pulldown resistors may be required on boot configuration pins.

5.1 Debug mode

In the Debugging mode, the CPU does not run. In this state, safely program the Flash memory via JTAG port.

To enter the debug mode, the boot configuration pins must be BTMODE [4:0] = “1xxx0” during reset.

NOTE : It the BTMODE[4] =0, the device will enter an undefined state. The pin must be set to 1 during reset.

5.2 Boot mode

At startup, BOOT pins are used to select one out of four boot operations:

- BTMODE [4:0] = “10001” : Boot from external NAND Flash(small 3C)
- BTMODE [4:0] = “10011” : Boot from external NAND Flash(small 4C)
- BTMODE [4:0] = “10101” : Boot from external NAND Flash(large 4C)
- BTMODE [4:0] = “10111” : Boot from external NAND Flash(large 5C)
- BTMODE [4:0] = “11001” : Boot from external NAND Flash(MLC 4bit)
- BTMODE [4:0] = “11011” : Boot from external NAND Flash(MLC 24bit)
- BTMODE [4:0] = “11101” : Serial Flash
- BTMODE [4:0] = “11111” : ROM / SRAM

6 Pin Mux

6.1 Pin Multiplexing Control Registers

Register	bit	1st	2nd	3rd	4th
		00	01	10	11
P0Mux(A) 0xF4000400	1:0	NF_D0	UART_TX1		GP0[0]
	3:2	NF_D1	UART_RX1		GP0[1]
	5:4	NF_D2	PWM_OUT1		GP0[2]
	7:6	NF_D3	CAP_IN1		GP0[3]
	9:8	NF_D4	UART_TX2		GP0[4]
	11:10	NF_D5	UART_RX2		GP0[5]
	13:12	NF_D6	PWM_OUT2		GP0[6]
	15:14	NF_D7	CAP_IN2		GP0[7]
P1Mux(B) 0xF4000404	1:0	NF_CS#			GP1[0]
	3:2	NF_ALE			GP1[1]
	5:4	NF_CLE			GP1[2]
	7:6	NF_WE#			GP1[3]
	9:8	NF_RE#			GP1[4]
	11:10	NF_BUSY#			GP1[5]
	13:12	UART_TX0			GP1[6]
	15:14	UART_RX0			GP1[7]
P2Mux(C) 0xF4000408	1:0	SDHC_D0	UART_TX3		GP2[0]
	3:2	SDHC_D1	UART_RX3		GP2[1]
	5:4	SDHC_D2	PWM_OUT3		GP2[2]
	7:6	SDHC_D3	CAP_IN3		GP2[3]
	9:8	SDHC_CLK			GP2[4]
	11:10	SDHC_CMD			GP2[5]
	13:12	PWM_OUT0			GP2[6]
	15:14	CAP_IN0	SRAM_CS1#		GP2[7]
P3Mux(D) 0xF400040C	1:0	I2S_CDCLK0			GP3[0]
	3:2	I2S_TX_SCLK0			GP3[1]
	5:4	I2S_TX_WS0			GP3[2]
	7:6	I2S_SDO0			GP3[3]
	9:8	I2S_SDI0			GP3[4]
	11:10	I2S_RX_SCLK0			GP3[5]
	13:12	I2S_RX_WS0			GP3[6]
	15:14	ICE_VCLK			GP3[7]
P4Mux(E) 0xF4000410	1:0	ICE_VDIN0	I2S_CDCLK1		GP4[0]
	3:2	ICE_VDIN1	I2S_TX_SCLK1		GP4[1]
	5:4	ICE_VDIN2	I2S_TX_WS1		GP4[2]
	7:6	ICE_VDIN3	I2S_SDO1		GP4[3]
	9:8	ICE_VDIN4	I2S_SDI1		GP4[4]
	11:10	ICE_VDIN5	I2S_RX_SCLK1		GP4[5]
	13:12	ICE_VDIN6	I2S_RX_WS1		GP4[6]
	15:14	ICE_VDIN7	EIRQ0		GP4[7]
P5Mux(F) 0xF4000014	1:0	SPI_CS0#	UART_TX3		GP5[0]
	3:2	SPI_SCK0	UART_RX3		GP5[1]
	5:4	SPI_MISO0	PWM_OUT3		GP5[2]
	7:6	SPI_MOSI0	CAP_IN3		GP5[3]
	9:8	TWI_SCL			GP5[4]
	11:10	TWI_SDA			GP5[5]
	13:12	SF_CS#			GP5[6]
	15:14	SF_CLK			GP5[7]
P6Mux(G) 0xF4000418	1:0	SF_D0			GP6[0]
	3:2	SF_D1			GP6[1]
	5:4	SF_D2			GP6[2]
	7:6	SF_D3			GP6[3]
	9:8	SRAM_WE#			GP6[4]
	11:10	SRAM_RE#			GP6[5]
	13:12	SRAM_BE1#			GP6[6]
	15:14	SRAM_CS0#			GP6[7]
P7Mux(H) 0xF400041C	1:0	SRAM_A0			GP7[0]
	3:2	SRAM_A1			GP7[1]
	5:4	SRAM_A2			GP7[2]
	7:6	SRAM_A3			GP7[3]
	9:8	SRAM_A4			GP7[4]
	11:10	SRAM_A5			GP7[5]

	13:12	SRAM_A6			GP7[6]
	15:14	SRAM_A7			GP7[7]
P8Mux(I) 0xF4000420	1:0	SRAM_A8	I2S_CDCLK1		GP8[0]
	3:2	SRAM_A9	I2S_TX_SCLK1		GP8[1]
	5:4	SRAM_A10	I2S_TX_WS1		GP8[2]
	7:6	SRAM_A11	I2S_SDO1		GP8[3]
	9:8	SRAM_A12	I2S_SDI1		GP8[4]
	11:10	SRAM_A13	I2S_RX_SCLK1		GP8[5]
	13:12	SRAM_A14	I2S_RX_WS1		GP8[6]
	15:14	SRAM_A15			GP8[7]
P9Mux(J) 0xF4000424	1:0	SRAM_D0			GP9[0]
	3:2	SRAM_D1			GP9[1]
	5:4	SRAM_D2			GP9[2]
	7:6	SRAM_D3			GP9[3]
	9:8	SRAM_D4			GP9[4]
	11:10	SRAM_D5			GP9[5]
	13:12	SRAM_D6			GP9[6]
	15:14	SRAM_D7			GP9[7]
P10Mux(K) 0xF4000428	1:0	SRAM_D8	UART_TX2		GP10[0]
	3:2	SRAM_D9	UART_RX2		GP10[1]
	5:4	SRAM_D10	PWMOUT2		GP10[2]
	7:6	SRAM_D11	CAPIN2		GP10[3]
	9:8	SRAM_D12	SPI_CS1#		GP10[4]
	11:10	SRAM_D13	SPI_SCK1		GP10[5]
	13:12	SRAM_D14	SPI_MISO1		GP10[6]
	15:14	SRAM_D15	SPI_MOSI1		GP10[7]
P11Mux(L) 0xF400042C	1:0	SRAM_A16	BOOTMODE[0]		GP11[0]
	3:2	SRAM_A17	BOOTMODE[1]		GP11[1]
	5:4	SRAM_A18	BOOTMODE[2]		GP11[2]
	7:6	SRAM_A19	BOOTMODE[3]		GP11[3]
	9:8	SRAM_A20	BOOTMODE[4]		GP11[4]
	11:10	SRAM_A21	LCD_VCLKIN		GP11[5]
	13:12	SRAM_WAIT#			GP11[6]
	15:14	EIRQ0	LCD_VCLKOUT		GP11[7]
P12Mux(M) 0xF4000430	1:0	UART_TX1	USB_HOST_POW		GP12[0]
	3:2	UART_RX1	USB_HOST_CUR		GP12[1]
	5:4	PWM_OUT1	SRAM_CS2		GP12[2]
	7:6	CAP_IN1	SRAM_CS3		GP12[3]

7 Interrupt Controller

AMAZON-II has 44 interrupts from internal device such as TIMER, SPI, TWI, UART. and, support for 2-external interrupts.

7.1 Features

- 46 channel interrupts (2-external interrupts and 44-interal interrupts
- 5 operating configurations for external interrupts
- 2 operating configurations for internal interrupts
- Interrupt enable for each channel
- Interrupt masking for each channel
- Programmable interrupt priority

7.2 Function Description

Interrupt handling processes are following steps.

1. Each interrupts source requests to interrupt controller.
2. After choosing the interrupt according to Interrupt Enable Register, the interrupt controller stores the interrupt of Interrupt Pending Register.
3. After decide interrupt priority, the interrupt controller request to CPU.
4. If the CPU receive an interrupt request, CPU′s interrupt is disabled and reads interrupt vector address from interrupt vector table. After CPU reads the address, the CPU calls Interrupt Service Routine (ISR).
5. Executes ISR
6. After finish executing ISR, CPU removes Interrupt value in the Interrupt Pending Register by writing Vector value into Interrupt Pending Clear Register.
7. CPU′s interrupt is enabled after finish (return) ISR routine.

Nested Interrupt handling processes are following steps.

1. Each interrupts source requests to interrupt controller.
2. After choose the interrupt according to Interrupt Enable Register, the interrupt controller stores the interrupt of Interrupt Pending Register.
3. After decide interrupt priority, the interrupt controller request to CPU.
4. If the CPU receive an interrupt request, CPU′s interrupt is disabled and reads interrupt vector address from interrupt vector table. After CPU reads the address, the CPU calls Interrupt Service Routine (ISR).
5. In order to allow nested interrupt, CPU removes interrupt that is already stored into Interrupt Pending Register by writing correspond vector value to Interrupt Pending Clear Register. After that CPU′s interrupt is enabled by asm(″set 13″) instruction.
6. Executes ISR.
7. If interrupt are occurred during ISR execution, CPU allows the interrupt and then execute the corresponding ISR.
8. After finish the new ISR execution, CPU returns the old ISR and then continues to execute.
9. Finish the ISR.

7.2.1 Interrupt Vector and Priority

EIRQ0 has the highest priority. The size of interrupt address is 4-byte. because interrupt vector address is 32-bit addressing mode.

Table 7-1 Interrupt Vector & Priority

Vector No.	*Description*	*Vector Address*
63	Reserved	0x0000017C
62	gpio [14]	0x00000178
61	gpio [13]	0x00000174
60	gpio [12]	0x00000170
59	gpio [11]	0x0000016C
58	gpio [10]	0x00000168
57	gpio [9]	0x00000164
56	Reserved	0x00000160
55	Reserved	0x0000015C
54	Reserved	0x00000158
53	gpio [8]	0x00000154
52	timer capture over	0x00000150
51	Reserved	0x0000014C
50	gpio [7]	0x00000148
49	axi dma [5]	0x00000144
48	Reserved	0x00000140
47	axi dma [4]	0x0000013C
46	gpio [6]	0x00000138
45	Reserved	0x00000134
44	gpio [5]	0x00000130
43	mjpeg decoding end	0x0000012C
42	gpio [4]	0x00000128
41	Reserved	0x00000124
40	Reserved	0x00000120
39	ahb dma [3]	0x0000011C
38	mjpeg fifo fill	0x00000118
37	gpio [3]	0x00000114
36	uart [3]	0x00000110
35	timer [3]	0x0000010C
34	spi [1]	0x00000108
33	gpio [2]	0x00000104
32	Reserved	0x00000100
31	Reserved	0x000000FC
30	spi [0]	0x000000F8
29	I2s tx [0]	0x000000F4
28	Sdcard	0x000000F0
27	ahb dma [2]	0x000000EC
26	nand flash	0x000000E8
25	watch dog	0x000000E4
24	Reserved	0x000000E0
23	Reserved	0x000000DC
22	uart [2]	0x000000D8
21	i2s rx [0]	0x000000D4
20	usb host	0x000000D0
19	Twi	0x000000CC
18	usb device	0x000000C8
17	timer [2]	0x000000C4
16	Reserved	0x000000C0
15	Reserved	0x000000BC
14	uart [1]	0x000000B8
13	gpio [1]	0x000000B4
12	ice	0x000000B0
11	ahb dma [1]	0x000000AC
10	pmu	0x000000A8
9	timer [1]	0x000000A4
8		0x000000A0
7	axi dma [0]	0x0000009C
6	uart [0]	0x00000098
5	gpio [0]	0x00000094
4	Crtc	0x00000090
3	ahb dma[0]	0x0000008C

2	Reserved	0x00000088
1	timer [0]	0x00000084
0	external irq[0]	0x00000080

*[] indicates channel number.

7.2.2 External Interrupt (EIRQx)

External Interrupt receives 5 types of external interrupt by configuring EINTMOD register.

- In the Low Level Mode, Interrupt is occurred every system cycle during External Interrupt signal keeps “Low“.
- In the High Level Mode, Interrupt is occurred every system cycle during External Interrupt signal keeps “High“.
- In the Falling Edge Mode, Interrupt is occurred when External Interrupt signal changes “High“ to “Low“.
- In the Rising Edge Mode, Interrupt is occurred when External Interrupt signal changes “Low“ to “High“
- In the Any Edge Mode, Interrupt is occurred when External Interrupt signal changes “Low“ to “High“ or “High“ to “Low“.

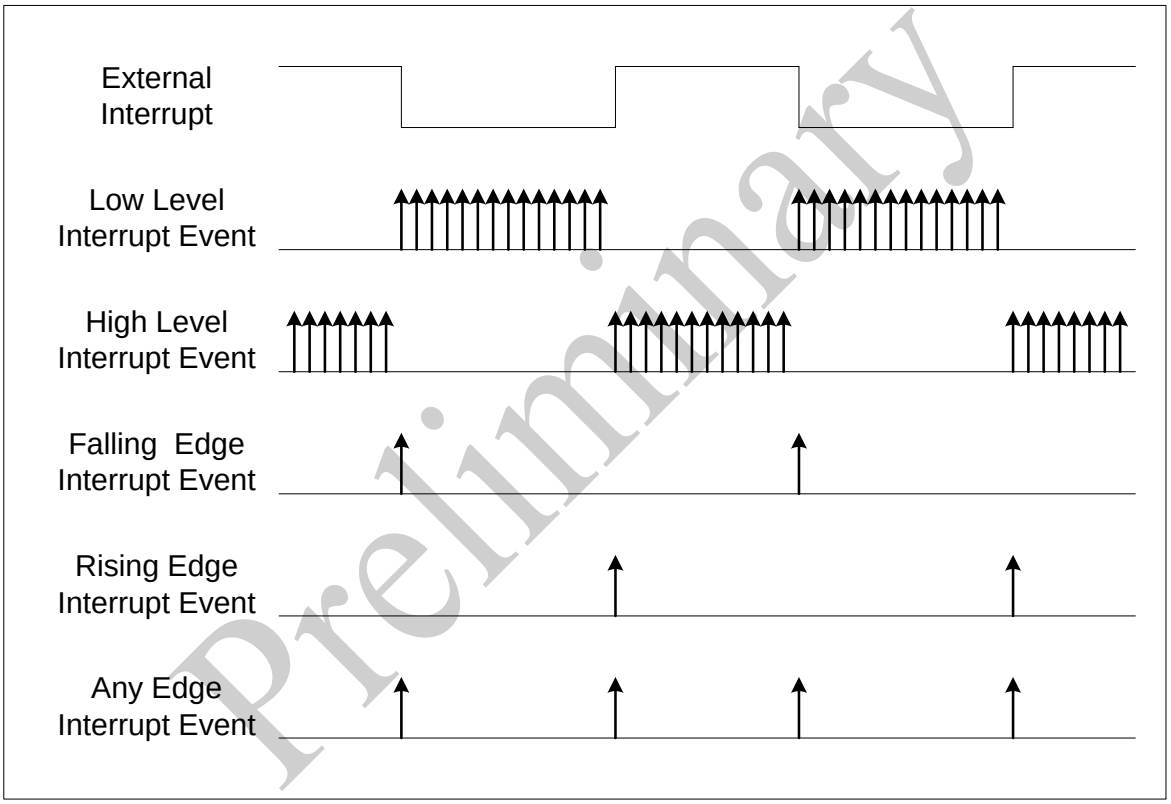


Figure 7-1 External Interrupt Mode

7.2.3 Internal Interrupt Mode

All of the internal interrupts are executed in “Rising Edge Mode”. However, if user wants to “High Level” interrupt handling, user can configures Internal Interrupt Mode Register.

7.2.4 Interrupt Pending and Interrupt Pending Clear

User can check interrupt status via Interrupt Pending Registers. An interrupt is stored into Interrupt Pending Register until be cleared by Interrupt Pending Clear Register. Also, if higher priority interrupt is stored in the Interrupt Pending Registers without Masking, the currently occurred interrupt is waiting for all of the higher priority interrupts are cleared.

In order to clear the interrupts that are stored in Interrupt Pending Registers, user should write the corresponding vector number into Interrupt Pending Clear Register.

7.2.5 Interrupt Enable

An interrupt, which is masked by Interrupt Mask Registers, is stored in Interrupt Pending Registers.
interrupt is stored in Interrupt Pending Register) However, an interrupt, which is disabled by Interrupt Enable Registers (IENR), is not stored in the Interrupt Pending Registers. Therefore, user can disable an interrupt that not allowed by using the registers (IENR).

7.2.6 Interrupt Mask Set/Clear Register

If the register is set, interrupt request is enable and, otherwise interrupt request is disabled.

CPU executes corresponding interrupt request by Interrupt Mask Registers. If the Interrupt Mask Set bit is 1, the interrupt controller requests the interrupt service to CPU. However, if the Interrupt Mask Clear bit is 1, the interrupt controller does not request the interrupt service to CPU.

Although, the Mask bit is 0, because an interrupt is stored into Interrupt Pending Registers (IPR), if user sets the Mask bit to 1, the interrupt controller requests interrupt service stored in Interrupt Pending Registers in the order of priority.

7.3 Register Description

7.3.1 Interrupt Pending Clear Register (INTPENDCLR)

Address : 0xF400_4800

Bit	*R/W*	*Description*	*Default Value*
31 : 8	R	Reserved	-
7 : 0	W	Interrupt Pending Register Clear Value (0x20 ~ 0x52)	0xFF

*** In order to clear Interrupt Pending Register, user should clear according to the Interrupt Vector No. (Refer to Interrupt Vector No.)

7.3.2 External Interrupt Mode and External PIN Level Register (EINTMOD)

Address : 0xF400_4804

Bit	*R/W*	*Description*	*Default Value*
31:4	R	Reserved	-
3	R	EIRQ0ST : EIRQ0 PIN Level	-
2 : 0	R/W	EIRQ0MOD : EIRQ0 Active State 000 : Low Level 001 : High Level 010 : Falling Edge 011 : Rising Edge 1xx : Any Edge	010

7.3.3 Internal Interrupt Mode Register (IINTMODn)

Address : 0xF400_4808 / 0xF400_4848

Bit	*R/W*	*Description*	*Default Value*
31	R/W	Vector No. 0x3F / 0x5F Interrupt Mode bit	0
30	R/W	Vector No. 0x3E / 0x5E Interrupt Mode bit	0
29	R/W	Vector No. 0x3D / 0x5D Interrupt Mode bit	0
28	R/W	Vector No. 0x3C / 0x5C Interrupt Mode bit	-
27	R/W	Vector No. 0x3B / 0x5B Interrupt Mode bit	0
26	R/W	Vector No. 0x3A / 0x5A Interrupt Mode bit	0
25	R/W	Vector No. 0x39 / 0x59 Interrupt Mode bit	0
24	-	Reserved	-
23	R/W	Vector No. 0x37 / 0x57 Interrupt Mode bit	0
22	R/W	Vector No. 0x36 / 0x56 Interrupt Mode bit	0
21	R/W	Vector No. 0x35 / 0x55 Interrupt Mode bit	0
20	R/W	Vector No. 0x36 / 0x54 Interrupt Mode bit	-
19	R/W	Vector No. 0x33 / 0x53 Interrupt Mode bit	0
18	R/W	Vector No. 0x32 / 0x52 Interrupt Mode bit	0
17	R/W	Vector No. 0x31 / 0x51 Interrupt Mode bit	0
16	-	Reserved	-
15	R/W	Vector No. 0x2F / 0x4F Interrupt Mode bit	0
14	R/W	Vector No. 0x2E / 0x4E Interrupt Mode bit	0
13	R/W	Vector No. 0x2D / 0x4D Interrupt Mode bit	0
12	R/W	Vector No. 0x2C / 0x4C Interrupt Mode bit	-
11	R/W	Vector No. 0x2B / 0x4B Interrupt Mode bit	0
10	R/W	Vector No. 0x2A / 0x4A Interrupt Mode bit	0
9	R/W	Vector No. 0x29 / 0x49 Interrupt Mode bit	0
8	-	Reserved	-
7	R/W	Vector No. 0x27 / 0x47 Interrupt Mode bit	0
6	R/W	Vector No. 0x26 / 0x46 Interrupt Mode bit	0
5	R/W	Vector No. 0x25 / 0x45 Interrupt Mode bit	0
4	R/W	Vector No. 0x24 / 0x44 Interrupt Mode bit	-
3	R/W	Vector No. 0x23 / 0x43 Interrupt Mode bit	0
2	R/W	Vector No. 0x22 / 0x42 Interrupt Mode bit	0
1	R/W	Vector No. 0x21 / 0x41 Interrupt Mode bit	0
0	-	Reserved	-

*** Internal Interrupt Mode bit
0 : High Level Mode
1 : Rising Edge Mode

7.3.4 Interrupt Pending Register (INTPENDn)

Address : 0xF400_480C / 0xF400_484C

Bit	*R/W*	*Description*	*Default Value*
31	R	Vector No. 0x3F / 0x5F Interrupt Pending bit	-
30	R	Vector No. 0x3E / 0x5E Interrupt Pending bit	-
29	R	Vector No. 0x3D / 0x5D Interrupt Pending bit	-
28	R	Vector No. 0x3C / 0x5C Interrupt Pending bit	-
27	R	Vector No. 0x3B / 0x5B Interrupt Pending bit	-
26	R	Vector No. 0x3A / 0x5A Interrupt Pending bit	-
25	R	Vector No. 0x39 / 0x59 Interrupt Pending bit	-
24	R	Vector No. 0x38 / 0x58 Interrupt Pending bit	-
23	R	Vector No. 0x37 / 0x57 Interrupt Pending bit	-
22	R	Vector No. 0x36 / 0x56 Interrupt Pending bit	-
21	R	Vector No. 0x35 / 0x55 Interrupt Pending bit	-
20	R	Vector No. 0x34 / 0x54 Interrupt Pending bit	-
19	R	Vector No. 0x33 / 0x53 Interrupt Pending bit	-
18	R	Vector No. 0x32 / 0x52 Interrupt Pending bit	-
17	R	Vector No. 0x31 / 0x51 Interrupt Pending bit	-
16	R	Vector No. 0x30 / 0x50 Interrupt Pending bit	-
15	R	Vector No. 0x2F / 0x4F Interrupt Pending bit	-
14	R	Vector No. 0x2E / 0x4E Interrupt Pending bit	-
13	R	Vector No. 0x2D / 0x4D Interrupt Pending bit	-
12	R	Vector No. 0x2C / 0x4C Interrupt Pending bit	-
11	R	Vector No. 0x2B / 0x4B Interrupt Pending bit	-
10	R	Vector No. 0x2A / 0x4A Interrupt Pending bit	-
9	R	Vector No. 0x29 / 0x49 Interrupt Pending bit	-
8	R	Vector No. 0x28 / 0x48 Interrupt Pending bit	-
7	R	Vector No. 0x27 / 0x47 Interrupt Pending bit	-
6	R	Vector No. 0x26 / 0x46 Interrupt Pending bit	-
5	R	Vector No. 0x25 / 0x45 Interrupt Pending bit	-
4	R	Vector No. 0x24 / 0x44 Interrupt Pending bit	-
3	R	Vector No. 0x23 / 0x43 Interrupt Pending bit	-
2	R	Vector No. 0x22 / 0x42 Interrupt Pending bit	-
1	R	Vector No. 0x21 / 0x41 Interrupt Pending bit	-
0	R	Vector No. 0x20 / 0x40 Interrupt Pending bit	-

*** Each bit of Interrupt Pending Register indicates the corresponding interrupt is occurred. The value of the Interrupt Pending Register is cleared by Interrupt Pending Clear Register. Generally, the interrupt is cleared when the interrupt request is finished.

.

7.3.5 Interrupt Enable Register (INTENn)

Address : 0xF400_4810 / 0xF400_4850

Bit	R/W	Description	Default Value
31	R/W	Vector No. 0x3F / 0x5F Interrupt Enable bit	0
30	R/W	Vector No. 0x3E / 0x5E Interrupt Enable bit	0
29	R/W	Vector No. 0x3D / 0x5D Interrupt Enable bit	0
28	R/W	Vector No. 0x3C / 0x5C Interrupt Enable bit	0
27	R/W	Vector No. 0x3B / 0x5B Interrupt Enable bit	0
26	R/W	Vector No. 0x3A / 0x5A Interrupt Enable bit	0
25	R/W	Vector No. 0x39 / 0x59 Interrupt Enable bit	0
24	R/W	Vector No. 0x38 / 0x58 Interrupt Enable bit	0
23	R/W	Vector No. 0x37 / 0x57 Interrupt Enable bit	0
22	R/W	Vector No. 0x36 / 0x56 Interrupt Enable bit	0
21	R/W	Vector No. 0x35 / 0x55 Interrupt Enable bit	0
20	R/W	Vector No. 0x34 / 0x54 Interrupt Enable bit	0
19	R/W	Vector No. 0x33 / 0x53 Interrupt Enable bit	0
18	R/W	Vector No. 0x32 / 0x52 Interrupt Enable bit	0
17	R/W	Vector No. 0x31 / 0x51 Interrupt Enable bit	0
16	R/W	Vector No. 0x30 / 0x50 Interrupt Enable bit	0
15	R/W	Vector No. 0x2F / 0x4F Interrupt Enable bit	0
14	R/W	Vector No. 0x2E / 0x4E Interrupt Enable bit	0
13	R/W	Vector No. 0x2D / 0x4D Interrupt Enable bit	0
12	R/W	Vector No. 0x2C / 0x4C Interrupt Enable bit	0
11	R/W	Vector No. 0x2B / 0x4B Interrupt Enable bit	0
10	R/W	Vector No. 0x2A / 0x4A Interrupt Enable bit	0
9	R/W	Vector No. 0x29 / 0x49 Interrupt Enable bit	0
8	R/W	Vector No. 0x28 / 0x48 Interrupt Enable bit	0
7	R/W	Vector No. 0x27 / 0x47 Interrupt Enable bit	0
6	R/W	Vector No. 0x26 / 0x46 Interrupt Enable bit	0
5	R/W	Vector No. 0x25 / 0x45 Interrupt Enable bit	0
4	R/W	Vector No. 0x24 / 0x44 Interrupt Enable bit	0
3	R/W	Vector No. 0x23 / 0x43 Interrupt Enable bit	0
2	R/W	Vector No. 0x22 / 0x42 Interrupt Enable bit	0
1	R/W	Vector No. 0x21 / 0x41 Interrupt Enable bit	0
0	R/W	Vector No. 0x20 / 0x40 Interrupt Enable bit	0

*** Interrupt Enable bit
0 : Interrupt Disable and Pending Clear
1 : Interrupt Enable

7.3.6 Interrupt Mask Status Register (INTMASKn)

Address : 0xF400_4814 / 0xF400_4854

Bit	R/W	Description	Default Value
31 : 0	R	Interrupt Mask Status Register 0 : Mask 1 : Unmask	0

*** Check all the status of the Mask

7.3.7 Interrupt Mask Set Register (INTMASKSETn)

Address : 0xF400_4814h / 0xF400_4854

Bit	R/W	Description	Default Value
31	W	Vector No. 0x3F / 0x5F Interrupt Mask Set bit	
30	W	Vector No. 0x3E / 0x5E Interrupt Mask Set bit	
29	W	Vector No. 0x3D / 0x5D Interrupt Mask Set bit	
28	W	Vector No. 0x3C / 0x5C Interrupt Mask Set bit	
27	W	Vector No. 0x3B / 0x5B Interrupt Mask Set bit	
26	W	Vector No. 0x3A / 0x5A Interrupt Mask Set bit	
25	W	Vector No. 0x39 / 0x59 Interrupt Mask Set bit	
24	W	Vector No. 0x38 / 0x58 Interrupt Mask Set bit	
23	W	Vector No. 0x37 / 0x58 Interrupt Mask Set bit	
22	W	Vector No. 0x36 / 0x56 Interrupt Mask Set bit	
21	W	Vector No. 0x35 / 0x55 Interrupt Mask Set bit	
20	W	Vector No. 0x34 / 0x54 Interrupt Mask Set bit	
19	W	Vector No. 0x33 / 0x53 Interrupt Mask Set bit	
18	W	Vector No. 0x32 / 0x52 Interrupt Mask Set bit	
17	W	Vector No. 0x31 / 0x51 Interrupt Mask Set bit	
16	W	Vector No. 0x30 / 0x50 Interrupt Mask Set bit	
15	W	Vector No. 0x2F / 0x4F Interrupt Mask Set bit	
14	W	Vector No. 0x2E / 0x4E Interrupt Mask Set bit	
13	W	Vector No. 0x2D / 0x4D Interrupt Mask Set bit	
12	W	Vector No. 0x2C / 0x4C Interrupt Mask Set bit	
11	W	Vector No. 0x2B / 0x4B Interrupt Mask Set bit	
10	W	Vector No. 0x2A / 0x4A Interrupt Mask Set bit	
9	W	Vector No. 0x29 / 0x49 Interrupt Mask Set bit	
8	W	Vector No. 0x28 / 0x48 Interrupt Mask Set bit	
7	W	Vector No. 0x27 / 0x47 Interrupt Mask Set bit	
6	W	Vector No. 0x26 / 0x46 Interrupt Mask Set bit	
5	W	Vector No. 0x25 / 0x45 Interrupt Mask Set bit	
4	W	Vector No. 0x24 / 0x44 Interrupt Mask Set bit	
3	W	Vector No. 0x23 / 0x43 Interrupt Mask Set bit	
2	W	Vector No. 0x22 / 0x42 Interrupt Mask Set bit	
1	W	Vector No. 0x21 / 0x41 Interrupt Mask Set bit	
0	W	Vector No. 0x20 / 0x40 Interrupt Mask Set bit	

*** Interrupt mask set bit
0 : No Effect
1 : Unmask : Pending interrupt is allowed to become active (interrupts sent to CPU).

7.3.8 Interrupt Masking Register (INTMASKn)

Address : 0xF400_4818 / 0xF400_4858

Bit	R/W	Description	Default Value
31	W	Vector No. 0x3F / 0x5F Interrupt Mask Clear bit	
30	W	Vector No. 0x3E / 0x5E Interrupt Mask Clear bit	
29	W	Vector No. 0x3D / 0x5D Interrupt Mask Clear bit	
28	W	Vector No. 0x3C / 0x5C Interrupt Mask. Clear bit	
27	W	Vector No. 0x3B / 0x5B Interrupt Mask Clear bit	
26	W	Vector No. 0x3A / 0x5A Interrupt Mask Clear bit	
25	W	Vector No. 0x39 / 0x59 Interrupt Mask Clear bit	
24	W	Vector No. 0x38 / 0x58 Interrupt Mask Clear bit	
23	W	Vector No. 0x37 / 0x57 Interrupt Mask Clear bit	
22	W	Vector No. 0x36 / 0x56 Interrupt Mask Clear bit	
21	W	Vector No. 0x35 / 0x55 Interrupt Mask Clear bit	
20	W	Vector No. 0x34 / 0x54 Interrupt Mask Clear bit	
19	W	Vector No. 0x33 / 0x53 Interrupt Mask Clear bit	
18	W	Vector No. 0x32 / 0x52 Interrupt Mask Clear bit	
17	W	Vector No. 0x31 / 0x51 Interrupt Mask Clear bit	
16	W	Vector No. 0x30 / 0x50 Interrupt Mask Clear bit	
15	W	Vector No. 0x2F / 0x4F Interrupt Mask Clear bit	
14	W	Vector No. 0x2E / 0x4E Interrupt Mask Clear bit	
13	W	Vector No. 0x2D / 0x4D Interrupt Mask Clear bit	
12	W	Vector No. 0x2C / 0x4C Interrupt Mask Clear bit	
11	W	Vector No. 0x2B / 0x4B Interrupt Mask Clear bit	
10	W	Vector No. 0x2A / 0x4A Interrupt Mask Clear bit	
9	W	Vector No. 0x29 / 0x49 Interrupt Mask Clear bit	
8	W	Vector No. 0x28 / 0x48 Interrupt Mask Clear bit	
7	W	Vector No. 0x27 / 0x47 Interrupt Mask Clear bit	
6	W	Vector No. 0x26 / 0x46 Interrupt Mask Clear bit	
5	W	Vector No. 0x25 / 0x45 Interrupt Mask Clear bit	
4	W	Vector No. 0x24 / 0x44 Interrupt Mask Clear bit	
3	W	Vector No. 0x23 / 0x43 Interrupt Mask Clear bit	
2	W	Vector No. 0x22 / 0x42 Interrupt Mask Clear bit	
1	W	Vector No. 0x21 / 0x41 Interrupt Mask Clear bit	
0	W	Vector No. 0x20 / 0x40 Interrupt Mask Clear bit	

*** Interrupt Mask bit
0 : No Effect
1 : Mask -> Pending interrupt is masked from becoming active (interrupts not sent to CPU).

7.3.9 Programmable Interrupt Priority Enable Register (PIPENR)

Address : 0xF400_481C

Bit	R/W	Description	Default Value
31 : 1	R	Reserved	-
0	R/W	Programmable Priority Enable bit 0 : Programmable Priority Disable 1 : Programmable Priority Enable	0

7.3.10 Interrupt Priority Vector n Register (IPVRn)

Address : 0xF400_4820 / 0xF400_4824 / 0xF400_4828 / 0xF400_482C / 0xF400_4830 / 0xF400_4834 / 0xF400_4838 / 0xF400_483C

Bit	R/W	Description	Default Value
31 : 28	R/W	8th Priority Interrupt Number	0x07
27 : 24	R/W	7th Priority Interrupt Number	0x06
23 : 20	R/W	6th Priority Interrupt Number	0x05
19 : 16	R/W	5th Priority Interrupt Number	0x04
15 : 12	R/W	4th Priority Interrupt Number	0x03
11 : 8	R/W	3rd Priority Interrupt Number	0x02
7 : 4	R/W	2nd Priority Interrupt Number	0x01
3 : 0	RW	1st Priority Interrupt Number	0x00

8 Serial Flash Memory Controller

Maximum capacity of Flash memory is 16Mbytes and maximum clock frequency is 80MHz. However Flash Memory Controller uses divided AHB Clock frequency. Due to that reason, Flash Memory operates half of the maximum frequency.

8.1 Feature

- Provides Single, Double, and Quad bit data transfer
- Provides Flash Erase and Flash Program in both H/W and S/W
- Provides XIP (eXecute In Place)

8.2 Function Description

8.2.1 Serial Flash Mode Register (SFMOD)

Determines Flash operation mode.
It can access flash data by Single, Dual and Quad bit size.

8.2.2 Serial Flash Baudrate Register (SFBRT)

Determines Flash Baud Rate.
It can configure width between high pulse and low pulse of clock frequency.

8.2.3 Serial Flash Chip Select High Pulse Width Register (SFCSH)

It determines deselect time of Chips select signal.
If the chips select signal is deselected, current status should not be changed.
After read operation, in the case of program tries to read, user keeps 50ns to access Status register after Erase or Program execution.
User connects external Flash memory to the AMAZON-II, the value of time is different according to flash type. Due to that reason, user should check the Flash deselect time.

8.2.4 Serial Flash Command Register (SFCMD)

Commands Chip Erase (C7h/60h), Power-down (B9h) and Release Power-down (ABh).

- Chip Erase (C7h/60h)
  - If user writes C7h or 60h to the register, entire flash data is erased.
- Power-Down (B9h)
  - If user writes B9h to the register, flash becomes power-down state after 3us (tDP).
  - ** (caution) Before power-down state, program should be executed in another memory space.
- Release Power-down (ABh)
  - If user writes ABh to the register, flash becomes stand-by state from power-down state after 3us (tRES1).

8.2.5 Serial Flash Status Register (SFSTS)

The register access the lowest 1byte of Flash status register.
It is used for checking bit0 (BUSY) that indicates write operation is finished or not.

8.2.6 Serial Flash 2nd Status Register for Winbond (SFSTS2/SFSTSW)

The register access the highest 1byte of Flash status register.
It is used for support Quad mode that can be done by setting bit1 (QE).

8.2.7 Serial Flash Sector/Block Erase Address Register (SFSEA/SFBEA)

With this register, user can erase flash in the unit of sector or block.
If user writes sector or block address to erase, the corresponding memory address is removed.

8.2.8 Serial Flash WIP Check Period Register (SFWCP)

This register determines the period of check in hardware, when user writes Flash such as program and erase. According to the value, Flash controller reads status register 0bit (BUSY). If the value of the bit is changed 1 into 0, the write operation is finished.

8.2.9 Serial Flash Clock Delay Register (SCKDLY)

8.2.10 Serial Flash Data Register (SFDAT)

The register is user for correction of Flash read timing.
User can delay read clock according to the value of the register.

8.3 Register Description

8.3.1 Serial Flash Mode Register (SFMOD)

Address : 0xF000_0000

Bit	*R/W*	*Description*	*Default Value*
31:9	R	Reserved	-
8	R/W	Chip select control 1: Chip select signal is controlled by H/W 0: Fix Chip select signal to Low Level	1b
7	R/W	Bus Error Enable 1: When user accesses to Flash in order to write, incurs Bus Error. 0: Allows Flash write access.	1b
6	R	Reserved	-
5	R	EQIO Mode Flag (Check Flash support) 1: EQIO Mode 0: Normal Mode If user writes EQIO (38h) to Command Register, Flash changes to EQIO mode.	0
4	R	Performance Enhance Mode (Check Flash support) 1: Applied Performance Enhance Mode 0: Normal Mode. If user enables Enhance Mode by writing 1 to FLPEM Register, It is enabled only when the Flash mode is Quad read or EQIO mode.	0
3	R/W	Bus Ready Control 0: Controls bus ready in case of write operation. S/W needs not check flash status. 1: After write operation, S/W checks flash status.	0b
2	R	Reserved	-
1:0	R/W	Flash Read Mode 00: Single Read Mode 01: Dual Read Mode 10: Quad Read Mode 11: Reserved	00b

8.3.2 Serial Flash Baudrate Register (SFBRT)

Address : 0xF000_0004

Bit	R/W	Description	Default Value
31:8	R	Reserved	-
7:4	R/W	SCK High Pulse Width 0000: 1clock 0001: 2clocks 0010: 3clocks … 1110: 15clocks 1111: 16clocks	111b
3:0	R/W	SCK Low Pulse Width 0000: 1clock 0001: 2clocks 0010: 3clocks … 1110: 15clocks 1111: 16clocks	111b

8.3.3 Serial Flash Chip Select High Pulse Width Register (SFCSH)

Address : 0xF000_0008

Bit	R/W	Description	Default Value
31:4	R	Reserved	-
3:0	R/W	Chip Select High Pulse Width 0000: 1clock 0001: 2clocks 0010: 3clocks … 1110: 15clocks 1111: 16clocks	Fh

8.3.4 Serial Flash Performance Enhance Mode Register (SFPEM)

Address : 0xF000_000C

Bit	R/W	Description	Default Value
31:1	R	Reserved	-
0	R/W	Performance Enhance Mode 1: Enable 0: Disable	0b

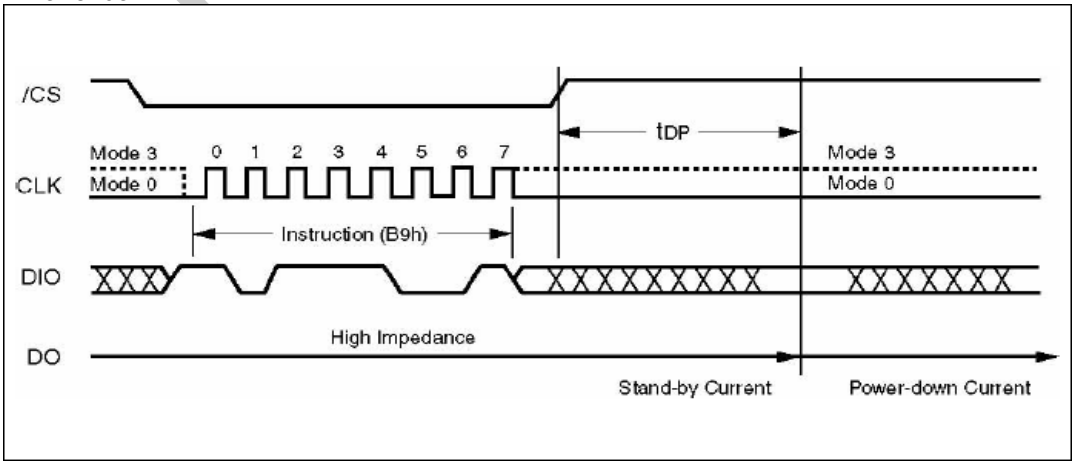
8.3.5 Serial Flash Command Register (SFCMD)

Address : 0xF000_0010

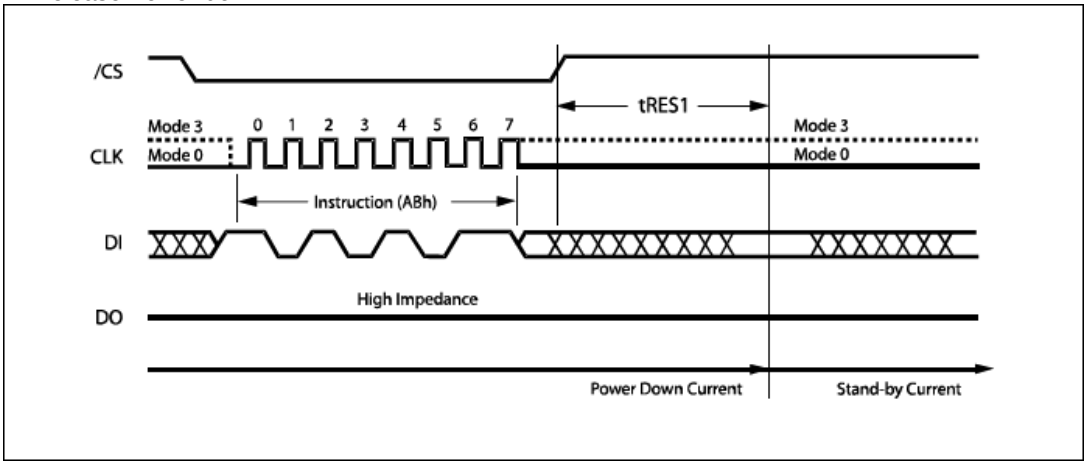
Bit	R/W	Description	Default Value
31:8	R	Reserved	-
7:0	R/W	Serial Flash Command	0b

- Chip Erase
  - If written C7h or 60h to this register, all area of flash erased.

- Power-down



- Release Power-down



8.3.6 Serial Flash Status Register (SFSTS)

Address : 0xF000_0014

Bit	R/W	Description	Default Value
31:8	R	Reserved	-
7	R/W	SRP(Status Register Protect) 1 : Status Register write disable 0 : Status Register write enable	0
6	R/W	WPDIS (#WP disable) 1 : WP# disable 0 : WP# enable	0
5	R	Reserved	0
4 : 2	R/W	Block Protect Configuration bit BP[2:0] Protect area Portion 000 : None 0/128 001 : Sector 0 to 125 126/128 010 : Sector 0 to 123 124/128 011 : Sector 0 to 119 120/128 100 : Sector 0 to 111 112/128 101 : Sector 0 to 95 96/128 110 : Sector 0 to 63 64/128 111 : All 128/128	000
1	R/W	WEL (Write Enable Latch) 1 : write enable 0 : write disable	0
0	R	WIP (Write In Progress) 1 : Write operation 0 : Not in write operation	0

8.3.7 Serial Flash Sector Erase Address Register (SFSEA)

Address : 0xF000_0018

Bit	R/W	Description	Default Value
31:24	R	Reserved	-
23:0	R/W	Serial Flash Sector Address to Erase	0b

8.3.8 Serial Flash Block Erase Address Register (SFBEA)

Address : 0xF000_001C

Bit	R/W	Description	Default Value
31:24	R	Reserved	-
23:0	R/W	Serial Flash Block Address to Erase	0b

8.3.9 Serial Flash Data Register (SFDAT)

Address : 0xF000_0020

Bit	R/W	Description	Default Value
31:0	R/W	Serial Flash Data (8, 16t, 32-bit supported)	0b

8.3.10 Serial Flash WIP Check Period Register (SFWCP)

Address : 0xF000_0024

Bit	R/W	Description	Default Value
31:0	R/W	Serial Flash WIP Status Check Period	FFFh

8.3.11 Serial Flash Clock Control Register (SCKDLY)

Address : 0xF000_0028

Bit	R/W	Description	Default Value
31:4	R	Reserved	-
3:0	R/W	Serial Flash Feedback Clock Delay Value 0 : 1 step delay 1 : 2 step delay … 15 : 16 step delay	0b

8.3.12 Serial Flash 2nd Status Read Register (SFSTS2)

Address : 0xF000_002C

Bit	R/W	Description	Default Value
7:0	R	Serial Flash 2nd Status (Winbond only)	0b

8.3.13 Serial Flash Status Write Register (SFSTSW)

Address : 0xF000_002C

Bit	R/W	Description	Default Value
15:0	W	Serial Flash Status to Write (Winbond only)	-

8.3.14 Serial Flash ID Read Register (SFIDR)

Address : 0xF000_0030

Bit	R/W	Description	Default Value
31:24	W	Reserved	-
23:0	R	Serial Flash JEDEC ID Read	000000h

9 SRAM/NOR Memory Controller

9.1 Function Description

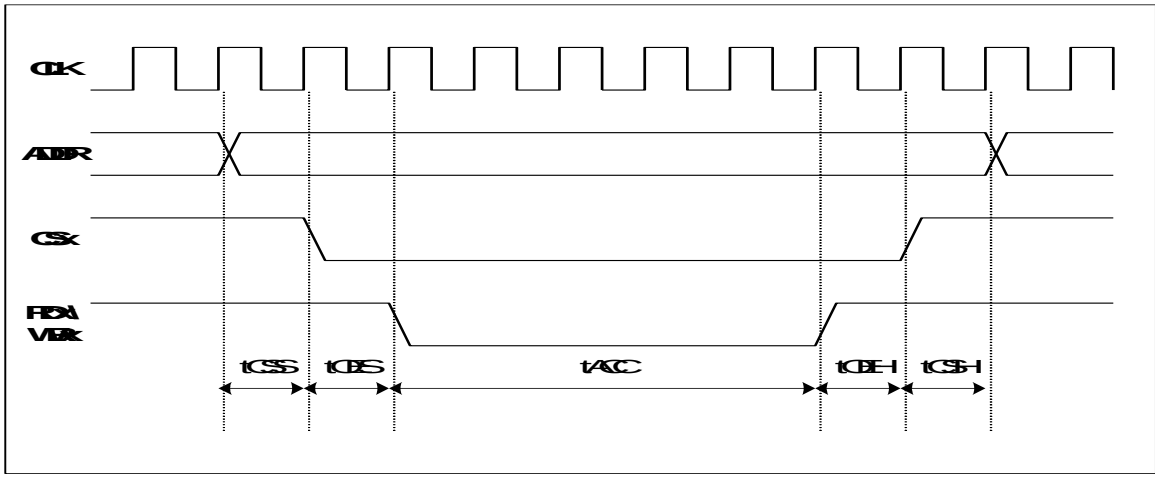
The AMAZON-II supports 8/16-bit external NOR Flash, PROM, and SRAM. In addition it supports 4 memories with maximum 4MB size.

9.2 Register Description

9.2.1 External SRAM CS0 Area Control Register (CSxCTRL)

Address : 0xF000_0400 / 0xF000_0404 / 0xF000_0408 / 0xF000_040C

Bit	*R/W*	*Description*	*Default Value*
31 : 16	R	Reserved	-
15 : 14	R/W	tCSS : Address Set-up before CSx 00 : 0 Clock 01 : 1 Clock 10 : 2 Clock 11 : 4 Clock	11
13 : 12	R/W	tOES : Chip Selection Set-up RDx / WRx 00 : 0 Clock 01 : 1 Clock 10 : 2 Clock 11 : 4 Clock	11
11 : 8	R/W	tACC : Access Cycle 0000 : 1 Clock 0001 : 2 Clock 0010 : 3 Clock 0011 : 4 Clock 0100 : 6 Clock 0101 : 8 Clock 0110 : 10 Clock 0111 : 12 Clock 1000 : 14 Clock 1001 : 16 Clock 1010 : 18 Clock 1011 : 20 Clock 1100 : 22 Clock 1101 : 24 Clock 1110 : 26 Clock 1111 : 30 Clock	1111
7 : 6	R/W	tOEH : Chip Selection Hold on RDx / WRx 00 : 0 Clock 01 : 1 Clock 10 : 2 Clock 11 : 4 Clock	11
5 : 4	R/W	tCSH : Address Holding Time after CSx 00 : 0 Clock 01 : 1 Clock 10 : 2 Clock 11 : 4 Clock	11
3	R/W	This bit determines whether using UBEx/LBEx pin for 16 bit Data bus 0 : UBEx/LBEx disabled 1 : UBEx/LBEx enabled	0
2	R/W	This bit determines WAIT status 0 : WAIT disabled 1 : WAIT enabled	0
1	R/W	This bit determines data bus width 0 : 8 bit 1 : 16 bit	0
0	R/W	Error Response Enable bit in Read only Memory 0 : Error Response Disable 1 : Error Response Enable	0



10 DDR2/mDDR Controller

10.1 Features

- Support 16bit DDR2, 16bit Mobile DDR SDRAM
- Support AXI Interface 32bit data width
- Support read data timing calibration
- 32byte FIFO for Tx/Rx data

10.2 Block Diagram

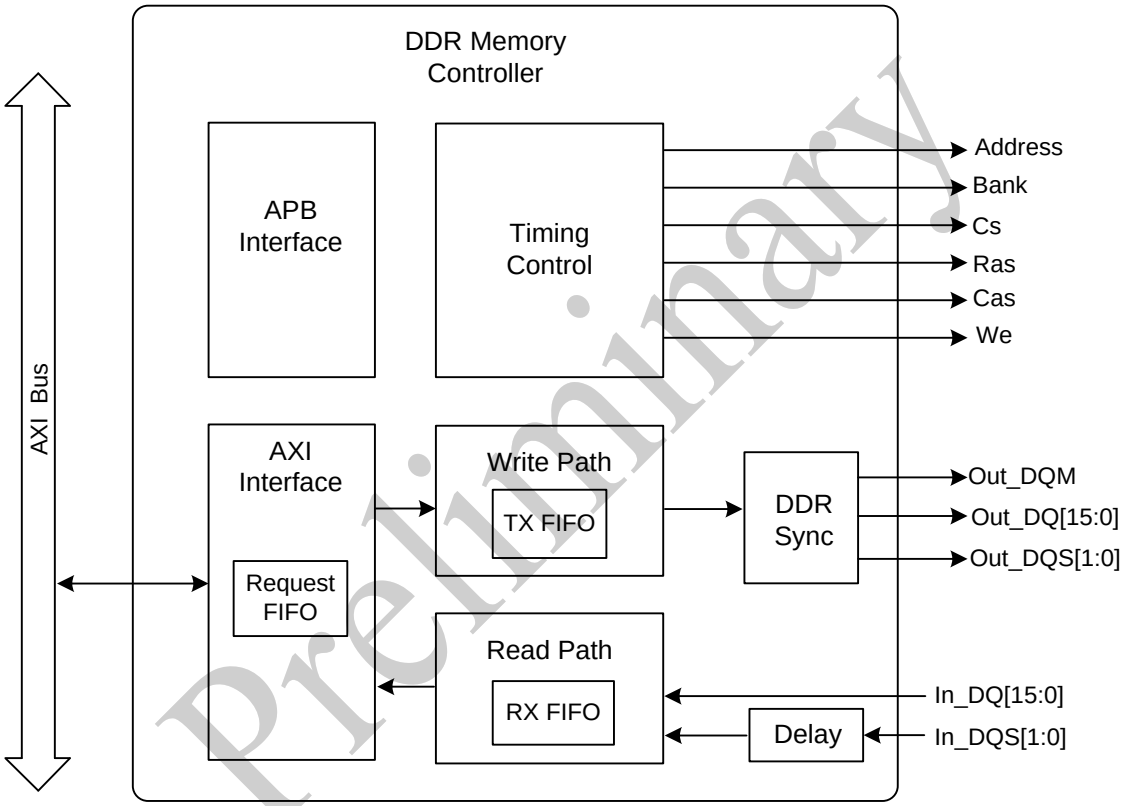


Figure 10-1 DDR2 Controller Block Diagram

10.3 Function Description

10.4 Register Description

10.4.1 DDR2 Control Register (DCR)

Address: 0xF400_0800

Bit	R/W	Description	Default Value
31 : 5	R	Reserved	-
9	R	Self refresh acknowledge 0 : no acknowledge 1 : acknowledge (self refresh mode starts)	0
8	W	Self refresh request 0 : normal mode 1 : self refresh request	0
7 : 5	R	Reserved	-
4	RW	Memory device selection 0 : ddr2 1 : mobile ddr	0
3 : 1	R	Reserved	-
0	RW	Memory Initialization start 0 : Disable 1 : Enable	0

10.4.2 DDR2 Address Size Register (DASR)

Address: 0xF400_0804

Bit	R/W	Description	Default Value
31 :10	R	Reserved	-
16	RW	Bank Size 0 : 2bit 1 : 3bit	0
15 : 10	R	Reserved	
9 : 8	RW	Row Address Size 00 : 12 bit 01 : 13 bit 10 : 14 bit 11 : 15 bit	00
7 : 2	R	Reserved	
1 : 0	RW	Column Address Size 00 : 8 bit 01 : 9 bit 10 : 10 bit	00

10.4.3 DDR2 Timing Configuration Register (DTCR)

Address: 0xF400_0808

Bit	R/W	Description	Default Value
31 : 13	R	Reserved	-
20	RW	Cas Latency margin	0
19 : 17	R	Reserved	-
16	RW	Write Recovery margin	0
15 : 13	R	Reserved	-
12	RW	Write Recovery cycle 0 : 4 cycle 1 : 3 cycle	0
11 : 10	R	Reserved	
9 : 8	RW	Refresh cycle ddr2 used / mobile ddr used 00 : 50 cycle / 00 : 24 cycle 01 : 30 cycle / 01 : 16 cycle 10 : 20 cycle / 10 : 10 cycle 11 : 16 cycle / 11 : 8 cycle	01
7 : 6	R	Reserved	0
5 : 4	RW	RAS latency 00 : 9 cycle 01 : 8 cycle 10 : 7 cycle 11 : 6 cycle	00
3 : 2	R	Reserved	
1 : 0	RW	CAS latency 00 : 1.5 cycle 01 : 2 cycle 10 : 2.5 cycle 11 : 3 cycle	11

10.4.4 DDR2 Refresh Rate Register (DRRR)

Address: 0xF400_080C

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
8	RW	Refresh Period Selection Register 0 : 7.8us period 1 : 15us period	0
7 : 0	RW	Memory Clock Frequency	0x85

10.4.5 DDR2 Glitch Control Register (DRRR)

Address: 0xF400_0810

Bit	R/W	Description	Default Value
31 : 21	R	Reserved	-
20	RW	DQS Preamble Margin When mDDR is running under 100Mhz	0
19 : 18	R	Reserved	-
17 : 16	RW	00 : 1/4 01 : 2/4 10 : 3/4 11 : 4/4	01
15 : 13	R	Reserved	-
12	RW 0 : Pull-Down Disable 1 : Pull-Down Enable		01
11 : 0	R	Reserved	-
8	RW	Removes glitch on the DQS signal in Postamble period. 0 : disable 1 : enable	0
7 : 6	R	Reserved	-
5 : 4	RW	(Only for mobile ddr) 00 : Full strength 01 : 1/2 strength 10 : 1/4 strength 11 : 1/8 strength	01
3	R	Reserved	-
2 : 0	RW	(Only for mobile ddr) 000 : Full strength 001 : 1/2 strength 010 : 1/4 strength 011 : 3/4 strength 100 : 3/4 strength 101 : reserved 110 : reserved 111 : reserved	001

10.4.6 DDR2 DQS Delay Register (DDDR)

Address: 0xF400_0814

Bit	R/W	Description	Default Value
31 : 0	RW	0x0000_0001 : 1 step delay 0x0000_0002 : 2 step delay 0x0000_0004 : 3 step delay 0x0000_0008 : 4 step delay : 0x4000_0000 : 31 step delay 0x8000_0000 : 32 step delay	0x00000100

10.4.7 DDR2 Preamble Delay Register (DPDR)

Address: 0xF400_0814

Bit	R/W	Description	Default Value
31 : 0	RW	0x0000_0001 : 1 step delay 0x0000_0002 : 2 step delay 0x0000_0004 : 3 step delay 0x0000_0008 : 4 step delay : 0x4000_0000 : 31 step delay 0x8000_0000 : 32 step delay	0x0000 0001

11 NAND Flash Controller

NAND Flash controls data transfer of 8-bit I/O NAND Flash Memory.

11.1 Features

- 8bit I/O support
- 3-cycle/4-cycle/5-cycle Address support
- 1bit for SLC and 4bit/24bit ECC for MLC
- Auto ECC Decoding support

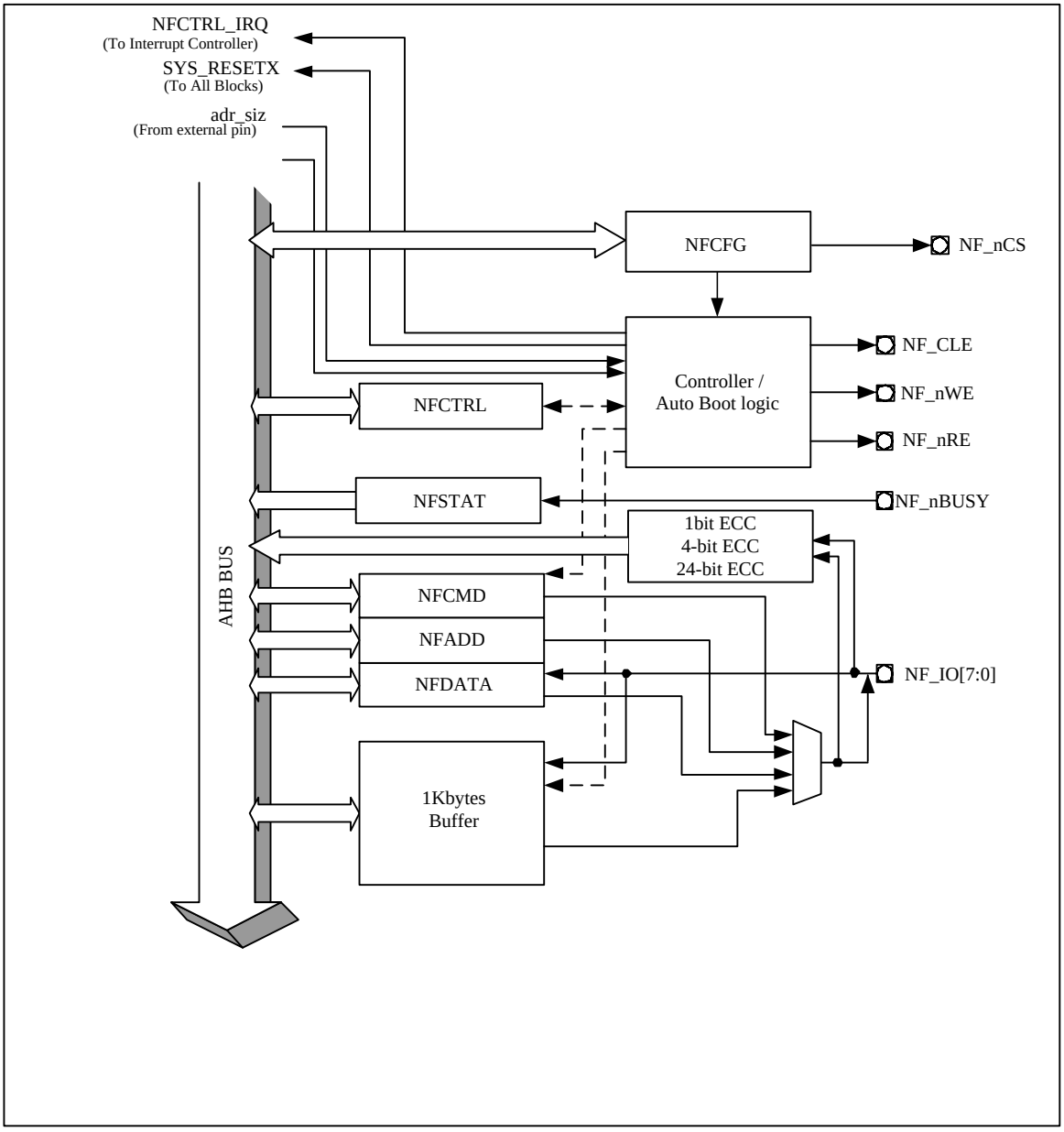


Figure 11-1 NAND Flash Controller Block Diagram

11.2 Function Description

11.2.1 Data Read/Write

1. Configures timing for data transfer to NFCFG register.
2. Configures NAND Flash Memory Command to NFCMD register.
3. Configures NAND Flash Memory address for access to NFADR register. At that time, repeatedly configures the register as Address cycle to NAND Flash access.
4. Operates Read/Write by NFCPUDATA. Before/After read data, user should check NDFL_nBUSY.

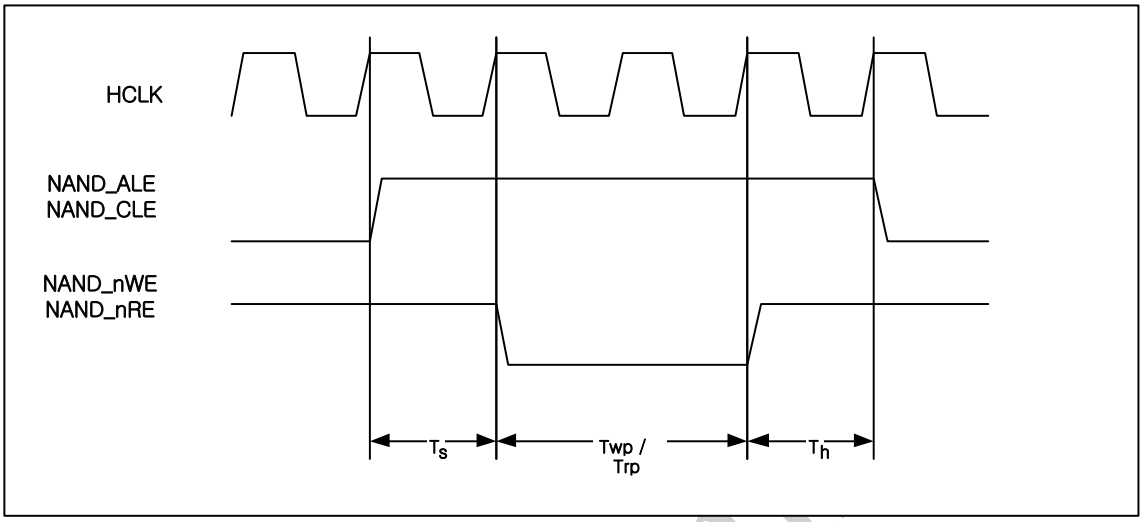


Figure 11-2 Read/Write Timing Diagram of NAND Flash Memory

11.2.2 DMA Operation

NAND Flash controller supports DMA Data Transfer. First of all, configures DMA Controller, then configures NAND Flash controller. If User configures DMA operation by NFCTRL register, NAND Flash Memory starts to DMA data transfer. In the case of the NAND Flash Memory is Large type (second generation), user can configures maximum 2Kbytes data transfer unit. In the case of the NAND Flash Memory is Small type (first generation), user can configures maximum 512Bytes for data transfer

11.3 ECC Operation

The AMAZON-II provides not only SLC type but also, MLC type NAND Flash. Because MLC type NAND Flash has higher error probability than SLC type, programmer should correct the error.

NAND Flash Controller generates Parity bit by using BCH algorithm. With the parity bit, the AMAZON-II can correct data error. The AMAZON-II provides error detection and error correction in 4-bit error for 512Bytes data and 24-bit error for 1Kbytes data.

11.3.1 ECC Encoding

1. After configures NFCFG register to use NAND Flash, Command and Address are sent.
2. After read NFECC1 register, clears ECC status and ECC registers.
3. Set ECC GEN bit of NFCTRL register to 1. (ECC Generation Enable)
4. Send 512Bytes or 1024Bytes data. Whenever data is transmitted, 52-bit or 336-bit Parity bits are generated and stored into NFECCn registers.
5. After finish sending data, reads the data in the order of NFECC0 register, NFECC1 register and stores into memory.
6. In order to continue to 512Bytes or 1024Bytes data transfer, repeats step 2~5.
7. If the1-page data transfer is finished, sets ECC GEN bit of NFCTRL register to 1. (ECC Generation disable)
8. Stores Parity bits of 512Bytes or 1024Bytes data in memory into spare space of NAND Flash.

11.3.2 ECC Decoding by S/W

1. After configures NFCFG register to use NAND Flash, Command and Address are sent.
2. After read NFECC1 register, clears ECC status and ECC registers.
3. Selects 4-bit or 24-bit ECC mode form NFCTRL register, then sets ECC GEN bit to 1. (ECC Decoding enable)
4. Reads 512Bytes or 1024Bytes data.
5. After read the data, accesses spare space and read parity bits.
6. After read the parity bits, automatically starts decoding. User can check the decoding is finished and succeeded by read NFSTAT register.
7. After finish decoding, NFERRLOC0~3 or NFERRLOC23 register holds error location, and NFERRPTN0~3 or NFERRPTN23 register holds 8-bit error pattern.
8. Correcting error data by Exclusive-OR Error location of NFERRLOCn register and error pattern of NFERRPTNn.
9. Repeats step 2~8 until finish reading 1-page

11.3.3 ECC Decoding by H/W (Auto ECC Decoding)

1. After configures NFCFG register to use NAND Flash, Command and Address are sent.
2. After read NFECC10 register, clears ECC status and ECC registers.
3. Selects 4-bit or 24-bit ECC mode from NFCTRL register, and set Auto ECC Decode bit to 1, then automatically reads data and parity from NAND Flash.
4. Check the Auto ECC Done bit of NFSTAT register is 1.
5. Reads error correction data from NFECD register
6. Repeats step 2~5 until finish reading 1-page.

11.4 Register Description

11.4.1 NAND Flash Memory Control Register (NFCTRL)

Address: 0xF000_0800

Bit	*R/W*	*Description*	*Default Value*
16	R/W	Auto ECC Enable bit 0: Auto ECC done 1: Auto ECC Start If the bit is set, Auto ECC is stated, and automatically clear when finished.	0
15	R/W	4-bit ECC Mode Set bit 0: 24-bit ECC Mode 1: 4-bit ECC Mode	1
14:13	R	Reserved	-
12	R/W	ECC Generation Enable bit 0 : Disable 1 : Enable	0
11	R/W	Endian Select bit 0 : Little Endian 1 : Big Endian	0
10	R/W	Data Swap Size 0 : 8bit 1 : 16bit	0
9	R/W	DMA Write Request bit 0 : DMA Write Request Clear 1 : DMA Write Request If the bit is set, DMA Transfer is stated, and automatically clear when finished.	0
8	R/W	DMA Read Request bit 0 : DMA Read Request Clear 1 : DMA Read Request If the bit is set, DMA Transfer is stated, and automatically clear when finished.	0
7	R/W	Busy End Interrupt Enable bit 0 : Interrupt Disable 1 : Interrupt Enable	0
6	R/W	DMA Clear Interrupt Enable bit 0 : Interrupt Disable 1 : Interrupt Enable	0
5	R/W	BCH ECC Decoding Done Interrupt Enable bit 0 : Interrupt Disable 1 : Interrupt Enable	0
4	R/W	Auto ECC Done Interrupt Enable bit 0 : Interrupt Disable 1 : Interrupt Enable	0
3:0	R/W	Reserved	0

11.4.2 NAND Flash Memory Command Set Register (NFCMD)

Address: 0xF000_0804

Bit	R/W	Description	Default Value
7 : 0	R/W	NAND Flash Memory Command	00h

11.4.3 NAND Flash Memory Address Register (NFADR)

Address: 0xF000_0808

Bit	R/W	Description	Default Value
7 : 0	R/W	NAND Flash Memory Address	00h

11.4.4 NAND Flash Memory Data Register (NFDATA)

Address: 0xF000_080C

Bit	R/W	Description	Default Value
31 : 0	R/W	NAND Flash Memory Read/Program Data 32/16/8-bit accessible	0000 0000h

11.4.5 NAND Flash Memory Operation Status Register (NFSTAT)

Address: 0xF000_0814

Bit	R/W	Description	Default Value
16:12	R	Error bit count The number of Error bit when ECC is finished.	0
11	R	Read data not FF Flag After erase, this bit is used for check all data for NAND Flash is 0xFF. If the read data is not 0xFF, this bit is set to 1. After read the register, this bit is cleared.	0
10	R	Reserved	-
9	R	DMA Write Done It is set when DMA Write is finished. After read the register, this bit is cleared.	0
8	R	DMA Read Done It is set when DMA Read is finished. After read the register, this bit is cleared.	0
7	R	BCH Decoding Done Status It is set when ECC Decoding is finished. After read the register, this bit is cleared.	0
6 : 4	R	Reserved	-
3	R	BCH Decoding Result 0 : Decoding Fail 1 : Decoding Success	0
2	R	Auto ECC Done bit If the value of the bit is set, it indicates Auto ECC is finished. After read the register, this bit is cleared.	0
1	R	NAND Flash Memory nBusy Level 0 : Busy 1 : Ready	nBUSY Level
0	R	NAND Flash Memory Busyx Rising Edge Status If Ready/Busyx signal changes low to high, this bit is set to 1. After read the register, this bit is cleared.	0

11.4.6 NAND Flash Memory ECC(Error Correction Code) Register (NFECC)

Address: 0xF000_0818

Bit	R/W	Description	Default Value
23 : 16	R/C	ECC2 (~P4, ~P4', ~P2, ~P2', ~P1, ~P1', ~P2048, ~P2048')	FFh
15 : 8	R/C	ECC1 (~P1024, ~P1024', ~P512, ~P512', ~P256, ~P256', ~P128, ~P128')	FFh
7 : 0	R/C	ECC0 (~P64, ~P64', ~P32, ~P32', ~P16, ~P16', ~P8, ~P8')	FFh

*** P1~P4 : Column Parity , P8~P2048 : Row Parity

*** ~ : Logically inverse operation

11.4.7 NAND Flash Memory Configuration Register (NFCFG)

Address: 0xF000_081C

Bit	R/W	Description	Default Value
20	R/w	Read data Latch timing Adjust bit. Configure as system clock. 0 : Minimum ~ 60Mhz 1 : 40Mhz ~ Maximum	1
19 : 17	R	Reserved	-
16	R/W	NDFL_nCS Control 0 : Chip Enable 1 : Chip Disable	1
15	R	Reserved	-
14 : 12	R/W	Ts : NDFL_ALE/NDFL_CLE Set-up Time 000 : 1 Clock 001 : 2 Clocks 010 : 3 Clocks 011 : 4 Clocks 100 : 5 Clocks 101 : 6 Clocks 110 : 7 Clocks 111 : 8 Clocks	111
11	R	Reserved	-
10 : 8	R/W	Twp : NDFL_nWE Pulse Width 000 : 1 Clock 001 : 2 Clocks 010 : 3 Clocks 011 : 4 Clocks 100 : 5 Clocks 101 : 6 Clocks 110 : 7 Clocks 111 : 8 Clocks	111
7	R	Reserved	-
6 : 4	R/W	Trp : NDFL_nRE Pulse Width 000 : 1 Clock 001 : 2 Clocks 010 : 3 Clocks 011 : 4 Clocks 100 : 5 Clocks 101 : 6 Clocks 110 : 7 Clocks 111 : 8 Clocks	111
3	R	Reserved	-
2 : 0	R/W	Th : NDFL_ALE/ NDFL_CLE/ NDFL_nCS Hold Time 000 : 1 Clock 001 : 2 Clocks 010 : 3 Clocks 011 : 4 Clocks 100 : 5 Clocks 101 : 6 Clocks 110 : 7 Clocks 111 : 8 Clocks	111

11.4.8 NAND Flash Memory ECC Code for LSN data (NFECCL)

Address: 0xF000_0820

Bit	R/W	Description	Default Value
15 : 8	R	S_ECC1 (1, 1, 1, 1, 1, 1, ~P4_s, ~P4'_s)	FFh
7 : 0	R	S_ECC0 (~P2_s, ~P2'_s, ~P1_s, ~P1'_s, ~P16_s, ~P16'_s, ~P8_s, ~P8'_s)	FFh

*** P1_s~P4_s : Column Parity, P8_s~P16_s : Row Parity
*** ~ : Logically inverse operation

11.4.9 NAND Flash Memory Error Corrected Data Register (NFECD)

Address: 0xF000_0824

Bit	R/W	Description	Default Value
31 : 0	R	Automatically Error Corrected Data	-

11.4.10 NAND Flash Memory Spare Address Register (NFSPADR)

Address: 0xF000_0828

Bit	R/W	Description	Default Value
15 : 0	R/W	Spare address to access during Auto ECC	0000h

11.4.11 NAND Flash Memory MLC ECCn Register (NFECCn)

Address: 0xF000_082C / 0xF000_0830 / 0xF000_0834 / 0xF000_0838 / 0xF000_083C / 0xF000_0840 / 0xF000_0844 / 0xF000_0848 / 0xF000_084C / 0xF000_0850 / 0xF000_0854

Bit	R/W	Description	Default Value
31 : 0	R	4-bit ECC Parity Value 52-bit parity[31:0] / 52-bit parity[52:32] 24-bit ECC Parity Value 336-bit parity[31:0] , 336-bit parity[63:32], 336-bit parity[95:64] , 336-bit parity[127:96], 336-bit parity[159:128], 336-bit parity[191:160], 336-bit parity[223:192], 336-bit parity[255:224], 336-bit parity[287:256], 336-bit parity[319:288], 336-bit parity[335:320]	0000 0000h

11.4.12 NAND Flash Memory Error Location n Register (NFERRLOCn)

Address: 0xF000_0858 / 0xF000_085C / 0xF000_0860 / 0xF000_0864 / 0xF000_0868 / 0xF000_086C / 0xF000_0870 / 0xF000_0874 / 0xF000_0878 / 0xF000_087C / 0xF000_0880 / 0xF000_0884 / 0xF000_0888 / 0xF000_088C / 0xF000_0890 / 0xF000_0894 / 0xF000_0898 / 0xF000_089C / 0xF000_08A0 / 0xF000_08A4 / 0xF000_08A8 / 0xF000_08AC / 0xF000_08B0 / 0xF000_08B4

Bit	R/W	Description	Default Value
10 : 0	R	Error byte location 1st~24th	0000h

11.4.13 NAND Flash Memory Error Pattern n Register (NFERRPTNn)

Address: 0xF000_08B8 ~ 0xF000_0D14

Bit	R/W	Description	Default Value
7 : 0	R	Error byte pattern 1st~24th	00h

11.4.14 NAND Flash Memory ID Register (NFMID)

Address: 0xF000_0D18

Bit	R/W	Description	Default Value
31 : 0	R	NAND Flash ID	0000 0000h

12 SD/MMC Controller

12.1 Features

- Support SD (ver 2.0) / MMC (ver 3.31) cards
- Provides High Speed (50MHz)
- Supports 1bit/4bit data bus
- Supports DMA Transfer
- Embeds 64 byte FIFO
- 40-bit Command Register
- 136-bit Response Register

12.2 Block Diagram

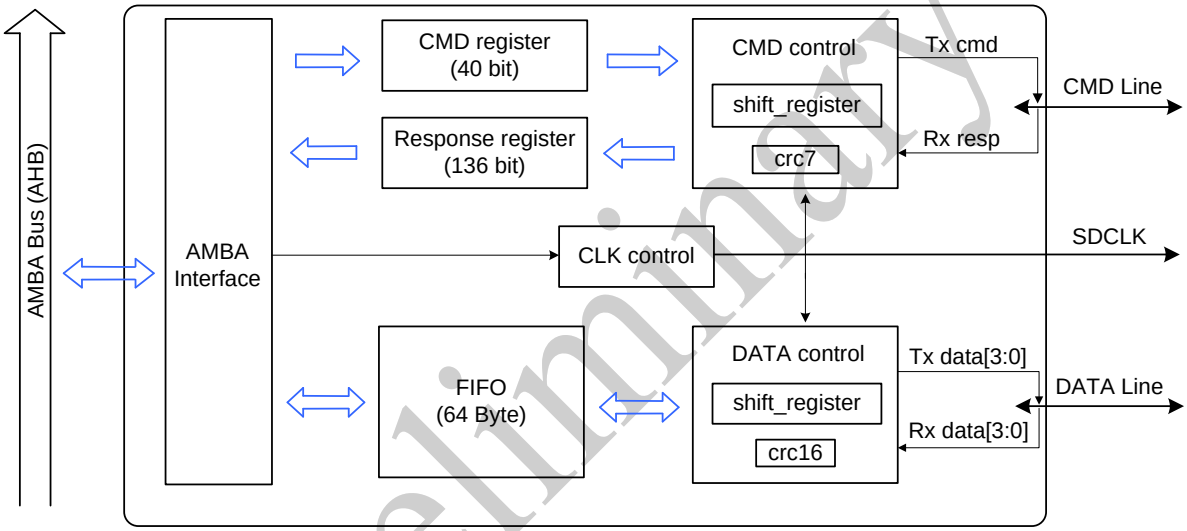


Figure 12-1 SDHC Block Diagram

12.3 SD Card Protocol

Communication between SD card and SD host is started with start bit and is stopped with stop bit based on Command, response, and data.

Command: Host (Controller) sends command line to SD card. The commands can be categorized as Broadcast command that transfers data to multiple SD card, and Addressed command that transfers data to one SD card.

Response: A response of host command. The selected SD card send the response with command line.

Data: The data is sent from SD card to SD card or from SD card to host with Data line in the unit of Block. Generally the block size is 512byte or 1024byte.

For reliability of data transfer, SD Card protocol checks Command, Response, and Data within CRC7 and CRC16. The CRC code generation and error detection is automatically done by H/W.

12.4 Register Description

12.4.1 SDHC Control Register (SDHCCON)

Address : 0xF000_0C00h

Bit	R/W	Description	Default Value
31 : 6	R	Reserved	-
5	R/W	MMC/SD HC Enable 0 : Disable (Controller is initialized) 1 : Enable Enable bit for HOST. If this bit is disabled, the status of controller is initialized and inside buffers are cleared.	0b
4 : 3	R/W	Memory access type 00 : byte align 01 : short align 10 : word align 11 : not use This bit determines alignment of data that stored in SD card.	00b
2	R/W	DMA mode selection 0 : Normal mode (data transfer by CPU) 1 : DMA mode (data transfer by DMA) Provides high speed data transfer via DMA.	0b
1	R/W	Bus width Selection 0 : 1bit data bus 1 : 4bit data bus	0b
0	R/W	MMC/SD clock enable 0 : Disable 1 : Enable	0b

12.4.2 SDHC Status Register (SDHCSTAT)

Address: 0xF000_0C04h

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	-
15	R	Card_Insertion 0 : No card insertion detection 1 : card insert detected This bit indicates that SD Card is inserted into a slot via Data line [3]. To use the bit, data line[3] should be connected with weak-pull-down resistance.	0b
14	R	Card_Removal 0 : No card removal detection 1 : card remove detected This bit indicates that SD Cared is removed from a slot via Data line [3].	0b
13	R	FIFO full This bit indicates 64-byte data FIFO is full or not.	0b
12	R	FIFO half full This bit indicates 64-byte data FIFO is half full.	0b
11	R	FIFO empty This bit indicates 64-byte data FIFO is empty.	1b
10	R/C	Command & response transaction done 0 : Command and response transaction is in progress 1 : Command and response transaction is done This bit informs that SD card received response when Host sent command. If the response does not reach, this bit is set to 1 by occurring Time out error.	0b
9	R/C	Data Write operation done 0 : Write operation is in progress or incomplete	0b

		1 : Write operation complete This bit informs that Data write operation is done. In the case of Data CRC error is occurred, the write operation is finished and then this bit is set to 1.	
8	R/C	Read operation done 0 : Read operation is in progress or incomplete 1 : Read operation complete This bit informs that Data write operation is done. In the case of Read Data CRC error is occurred, the read operation is finished and then this bit is set to 1.	0b
7 :6	R/C	Write CRC error code 00 : No CRC Error 01 : CRC Error (CRC error in data block) 10 : No CRC response (Ignored data block in SD card) 11 : Reserved During write operation, this bit informs CRC test result from SD Card. SD Card test CRC every time when Host sends one block data and send the result of CRC to the Host.	00b
5	R/C	Response CRC error 0 : No error 1 : Response CRC error occurred This bit informs CRC error occurred in response.	0b
4	R/C	Read data CRC error 0 : No error 1 : Read data CRC error occurred This bit informs that CRC error occurred in read data from SD Card.	0b
3	R/C	Write data CRC error 0 : No error 1 : Write data CRC error occurred This bit informs that CRC error occurred in write data to SD Card.	0b
2	R/C	Response time out error 0 : No error 1 : Command response was not received in time Specified This bit informs that command response is not received in time.	0b
1	R/C	Read data time out error 0 : No error 1 : The expected data from card was not received in time Specified This bit informs that read data from SD card is not received in time.	0b
0	R	Memory busy state 0 : Memory is ready 1 : Memory is busy This bit indicates busy status of SD Card.	0b

R/C indicates Read/Clear. In order to clear specific bit of status, writes 1 to corresponding bit.

Status [15:8] is an interrupt source. If one of the bits is set to 1, an interrupt is occurred and keeps requesting interrupt until the bit is cleared.

12.4.3 SDHC Clock Divide Register (SDHCCD)

Address : 0xF000_0C08h

Bit	R/W	Description	Default Value
31 : 10	R	Reserved.	-
9 : 0	R/W	MMC/SD clock Divide Register $f_{SDCLK} = \frac{f_{AHB\_Clock}}{2 + Divide\ [9:0]}$	200h

12.4.4 SDHC Response Time Out Register (SDHCRTO)

Address: 0xF000_0C0Ch

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7 : 0	R/W	Response time out. This register is configured in maximum wait time for response after sending command. If the response does not reach in the specified time, response time out error is occurred. The unit of time is based on the clock of SD Card, and if the last bit of command is transferred, the clock count begins. 01h : 1 clock count 02h : 2 clock counts ... FFh : 255 clock counts	FFh

12.4.5 SDHC Read Data Time Out Register (SDHCRDTO)

Address: 0xF000_0C10h

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	-
15 : 8	R/W	Data read time out. This register is configured in maximum wait time for read data after sending read command. User can configure upper 8-bit and lower 8-bit is fixed with 00h. Generally, FF00h is recommended.	FFh
7 : 0	R	Reserved.	00h

12.4.6 SDHC Block Length Register (SDHCBL)

Address: 0xF000_0C14h

Bit	R/W	Description	Default Value
31 : 12	R	Reserved	-
11 : 0	R/W	Block length. This register determines the size of data block.	200h

12.4.7 SDHC Number of Block Register (SDHCNOB)

Address: 0xF000_0C18h

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	-
15 : 0	R/W	This register specifies the number of blocks to transfer when using Multi-block command. Its value is decreased when one block is transferred and if the data transfer is finished, the value becomes 0.	0000h

12.4.8 SDHC Interrupt Enable Register (SDHCIE)

Address : 0xF000_0C1Ch

Bit	R/W	Description	Default Value
31 : 8		Reserved	-
7	R/W	Card insert detection Interrupt enable 0 : disable 1 : enable	0b
6	R/W	Card remove detection Interrupt enable 0 : disable	0b

		1 : enable	
5	R/W	FIFO full Interrupt enable 0 : disable 1 : enable	0b
4	R/W	FIFO half full Interrupt enable 0 : disable 1 : enable	0b
3	R/W	FIFO empty Interrupt enable 0 : disable 1 : enable	0b
2	R/W	End command response Interrupt enable 0 : disable 1 : enable	0b
1	R/W	Write operation done Interrupt enable 0 : disable 1 : enable	0b
0	R/W	Read operation done Interrupt enable 0 : disable 1 : enable	0b

SDHCSTAT [15:8] is an interrupt source, and SDHCIE register is an interrupt enable signal. If an interrupt is occurred, interrupt service routine is executed and sets to 0 in SDHCSTAT [15:8] according to the interrupt source. However, because card insert detection interrupt and card remove detection interrupt are not cleared in SDHCSTAT [15] and SDHCSTAT [14], interrupt enable bit is set to “0” in the interrupt service routine (Interrupt disable).

12.4.9 SDHC Command Control Register (SDHCCMDCON)

SDHCCMDCON register is used for sending command. Once user writes to SDHCCMDCON register, user command is sent to SD card as the register configuration.

Address: 0xF000_0C20h

Bit	*R/W*	*Description*	*Default Value*
31 : 11	R	Reserved	-
10	R/W	This bit determines that a command type needs response or not. In the case of the configuration is No response, response does not be stored into response buffer. 0 : no response 1 : wait response	0b
9 : 8	R/W	This bit determines response type. Because the response type can be changed according to the command, user should select the right response type. 00 : short response (response size : 48bit) 01 : short response with busy (response size : 48bit ,) 10 : long response (response size : 136bit)	00b
7	R/W	This bit determines a command uses data stream or not. In the case of read command or write command, this bit should be 1. 0 : without data 1 : with data	0b
6	R/W	This bit determines a direction of Data FIFO In/Out. In the case of read command, the bit is set to 0. In the case of write command, the bit is set to 1. 0 : read data 1 : write data	0b
5 : 0	R/W	This bit specifies command number. The command number of MMC and SD card is different. Refer to MMC and SD Card specification. 00h = CMD0 01h = CMD1 ... 3Fh = CMD63	00h

12.4.10 SDHC Command Argument Register (SDHCCMDA)

Address: 0xF000_0C24h

Bit	R/W	Description	Default Value
31 : 0	R/W	Command argument. It configures argument of command token.	0000 0000h

12.4.11 SDHC Response FIFO Access Register (SDHCRFA)

Address: 0xF000_0C28h

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	-
15 : 0	R/W	FIFO size to store response. the size is 8x16 bit.	0000h

12.4.12 SDHC Data FIFO Access Register (SDHCDFA)

Address: 0xF000_0C2Ch

Bit	R/W	Description	Default Value
31 : 0	R/W	Data FIFO size. (16x32bit)	-

13 USB Device

USB Device of the Amzon2 supports 2.0 Full-speed (12Mbps) and consists of 5 endpoints.

USB Protocol is supported in hardware, and provides automatically data retry, data toggle, and power management (suspend and resume). The USB device includes PHY.

13.1 Features

- Supports USB 2.0 Full Speed(12Mbps)
- Supports 5 Endpoint
- Supports suspend and resume signaling

Table 13-1 Endpoint List

Endpoint	*Max Size (bytes)*	*Direction*	*Transaction Type*
0	16	IN/OUT	Control
1	64	OUT	Bulk
2	64	IN	Bulk
3	16	OUT	Interrupt
4	16	IN	Interrupt

13.2 Register Summary

Table 13-2 USB Core Register List

Register	*Address*	*R/W*	*Description*	*Default Value*
USBFA	0xF0001000	R/W	Function address register	0x00
USBPM	0xF0001004	R/W	Power management register	0x00
USBEPI	0xF0001008	R/W	Endpoint interrupt register	0x00
USBINT	0xF0001010	R/W	USB interrupt register	0x00
USBEPIEN	0xF0001014	R/W	Endpoint interrupt enable register	0x1F
USBINTEN	0xF0001018	R/W	USB interrupt enable register	0x04
USBLBFN	0xF000101C	R	Frame number1 register	0x00
USBHBFN	0xF0001020	R	Frame number2 register	0x00
USBIND	0xF0001024	R/W	Index register	0x00
USBMP	0xF0001028	R/W	MAXP register	0x00
USBEP0C	0xF000102C	R/W	EP0 control register	0x00
USBIC1	0xF000102C	R/W	EP2, 4 IN Control register1	0x00
USBIC2	0xF0001030	R/W	EP2, 4 IN Control register2	0x00
USBOC1	0xF0001038	R/W	EP1, 3 OUT Control register 1	0x00
USBOC2	0xF000103C	R/W	EP1, 3 OUT Control register 2	0x00
USBLBOWC	0xF0001040	R	Low Byte OEP Write count register	0x00
USBHBOWC	0xF0001044	R	High Byte OEP write count register	0x00
USBEP0D	0xF0001048	R/W	EP0 FIFO data register	0x00
USBEP1D	0xF000104C	R/W	EP1 FIFO data register	0x0000_0000
USBEP2D	0xF0001050	R/W	EP2 FIFO data register	0x0000_0000
USBEP3D	0xF0001054	R/W	EP3 FIFO data register	0x00
USBEP4D	0xF0001058	R/W	EP4 FIFO data register	0x00

13.2.1 USB Function Address Register

USBFAR register holds USB Device address that is assigned by host. MCU stores the data to the register by executing SET_ADDRESS Descript. This value is used for next token.

13.2.2 USB Power Management Register

Power management register is used by Suspend, Resume and Reset signals. Statuses of Suspend and Reset are stored into USB_INTERRUPT register.

13.2.3 USB Interrupt Registers

This register informs statuses of USB Host request and Endpoint.

13.2.4 USB Interrupt Enable Registers

Interrupt enables of each endpoint. Most of interrupts are enabled initially, but suspend interrupt is disabled.

13.2.5 Frame Number Registers

This register holds frame number at the end of frame packet.

13.2.6 Index Register

The index register is used for selecting control register of each endpoint.

13.2.7 MAXP Register

User can configure FIFO size that is times of 8byte. However, user cannot set larger the FIFO size than maximum FIFO size that is provided by each endpoint.

13.2.8 EP0 Control Register

This register represents control and status of Endpoint0.

13.2.9 IN Control Registers

This register represents control and status of IN Endpoint

13.2.10 Out Control Registers

This register represents control and status of OUT Endpoint

13.2.11 Out Write Count Registers

The 2 Out Write Count registers hold write count. The registers hold the number of packets that are used by MCU, if OPOPR bit is set at the OUT endpoint.

13.2.12 Endpoint FIFO Access Registers

The register accesses to an Endpoint FIFO.

13.3 Register Description

13.3.1 USB Function Address Register (USBFA)

Address : 0xF000_1000h

Bit	R/W		Description	Default Value
	MCU	USB		
31 : 8			Reserved	
7	R/W	R/ Clear	ADDUP: ADDR_UPDATE bit. The MCU sets this bit whenever it updates the FUNCTION_ADDR field in this register. The FUNCTION_ADDR field is used after the Status phase of a Control transfer, which is signaled by the clearing of the DATA_END bit in the Endpoint 0 CSR.	0
6 : 0	R/W	R	FUNADD: FUNCTION_ADDR bits. MCU writes address into this bit.	0

13.3.2 USB Power Management Register (USBPM)

Address : 0xF000_1004h

Bit	R/W		Description	Default Value
	MCU	USB		
31 : 4			Reserved	
3	R	Set	UBRST: USB_RESET bit. If USB receives Reset signal from host, USB sets this bit. If the Reset signal remains in bus, this bit keeps holding 1.	0
2	W/R	R	UBRSUM: USB_RESUME bit. In order to initialize Resume signal, MCU configures this bit during 10ms (Max 15ms). In the Suspend mode, USB generates Resume signal during this bit is set.	0
1	R	R/W	UBSPDMOD: SUSPEND_MODE bit. USB configures this bit when enters into Suspend mode. This bit is cleared by following conditions. - MCU clears MCU_RESUME to finish Resume signal. - MCU reads interrupt register 3 when USB_RESUME interrupt is occurred.	0
0	R/W	R	UBENSPD : ENABLE_SUSPEND bit = 1 Enable Suspend mode = 0 Disable Suspend mode (Default) If this bit is set to 0, USB Device does not enter suspend mode.	0

13.3.3 USB Endpoint Interrupt Register (USBEPI)

Address : 0xF000_1008h

Bit	R/W		Description	Default Value
	MCU	USB		
31 : 5			Reserved	
4	R/ Clear	Set	EP4INT: EP4 Interrupt bit. (Interrupt in mode) This bit is for Endpoint4 interrupt. (Refer to USBIC1R, USBIC2R bit) When ICIPR(In Control 1 In Packet Ready bit) bit is cleared When FIFO is flushed. When ICSTSTAL (In Control 1 Sent Stall bit) bit is set.	0
3	R/ Clear	Set	EP3INT: EP3 Interrupt bit. (Interrupt out mode) This bit is for Endpoint3 interrupt. (Refer to USBOC1R, USBOC2R bit) When OCOPR (Out Control 1 Out Packet Ready bit) bit is set. When OCSTSTAL (Out Control 1 Sent Stall bit) bit is set.	0
2	R/ Clear	Set	EP2INT: EP2 Interrupt bit. (Bulk in mode) This bit is for Endpoint2 interrupt. (Refer to USBIC1R, USBIC2R bit) When ICIPR (In Control 1 In Packet Ready bit) bit is clear. When FIFO is flushed. When ICSTSTAL (In Control 1 Sent Stall bit) bit is set.	0

1	R/ Clear	Set	EP1INT: EP1 Interrupt bit. (Bulk out mode) This bit is for Endpoint1 interrupt. (Refer to USBOC1R, USBOC2R bit) When OCOPR (Out Control 1 Out Packet Ready bit) bit is set. When OCSTSTAL (Out Control 1 Sent Stall bit) bit is set.	0
0	R/ Clear	Set	EP0INT: EP0 Interrupt bit. (Control mode) This bit is for Endpoint0 interrupt. (Refer to USBEP0CR bit) EP0OPR bit is set. EP0IPR bit is cleared EP0STSTAL bit is set EP0STED bit is set EP0DED bit is cleared(Indicates End of control transfer)	0

13.3.4 USB Interrupt Register (USBINT)

Address : 0xF000_1010h

Bit	R/W		Description	Default Value
	MCU	USB		
31 : 3			Reserved	
2	R/ Clear	Set	RSTINT: USB Reset Interrupt bit. USB set this bit when receives Reset signal.	0
1	R/ Clear	Set	RSUMINT: Resume Interrupt bit. In the suspend mode, USB set this bit when receives Resume signal. If the resume is caused by USB Reset, MCU interrupt is occurred by Resume interrupt. If clock continues to operate and duration of SE0 status is 3ms, then USB Reset interrupt is occurred.	0
0	R/ Clear	Set	SPDINT : Suspend Interrupt bit USB sets this bit when receive suspend signal. If there are no operations in bus during 3ms, this bit is set. Therefore, if the MCU does not stop Clock after the first suspend interrupt, the interrupt is occurred every 3ms. The default value of this interrupt is disable.	0

13.3.5 Endpoint Interrupt Enable Register (USBEPIEN)

Address : 0xF000_1014h

Bit	R/W	Description	Default Value
31 : 5	R	Reserved	
4	R/W	EP4INTEN : Endpoint 4 Interrupt enable bit	1
3	R/W	EP3INTEN : Endpoint 3 Interrupt enable bit	1
2	R/W	EP2INTEN : Endpoint 2 Interrupt enable bit	1
1	R/W	EP1INTEN : Endpoint 1 Interrupt enable bit	1
0	R/W	EP0INTEN : Endpoint 0 Interrupt enable bit	1

13.3.6 USB Interrupt Enable Register (USBINTEN)

Address : 0xF000_1018h

Bit	R/W	Description	Default Value
31 : 3	R	Reserved	
2	R/W	RSTINTEN : USB RESET Interrupt enable bit	1
1	R	Reserved	
0	R/W	SPDINTEN : SUSPEND Interrupt enable bit	0

13.3.7 USB Low Byte Frame Number Register (USBLBFN)

Address : 0xF000_101Ch

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	
7 : 0	R/W	Frame Number 1 register	0x00

13.3.8 USB High Byte Frame Number Register (USBHBFN)

Address : 0xF000_1020h

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	
7 : 0	R/W	Frame Number 2 register	0x00

13.3.9 USB Index Register (USBIND)

Address : 0xF000_1024h

Bit	R/W	Description	Default Value
31 : 3	R	Reserved	
2 : 0	R/W	Index register 000 : Endpoint 0 001 : Endpoint 1 010 : Endpoint 2 011 : Endpoint 3 100 : Endpoint 4 101 : Reserved 110 : Reserved 111 : Reserved	000

13.3.10 USB MAXP Register (USBMP)

Address : 0xF000_1028h

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	
7 : 0	R/W	Max FIFO Size 0000_0001 MAXP=8 0000_0010 MAXP=16 0000_0100 MAXP=32 0000_0C00 MAXP=64	0x00

13.3.11 USB EP0 Control Register (USBEP0C)

Address : 0xF000_102Ch

Bit	R/W		Description	Default Value
	MCU	USB		
7	Clear		EP0SUEC : EP0 Set Up End Clear bit. MCU write 1 to this bit in order to clear EP0STED bit.	0
6	Clear		EP0OPRC : EP0 Out Packet Ready Clear bit. MCU write 1 to this bit in order to clear EP0OPR bit.	0
5	Set	Clear	EP0SDSTAL: EP0 Send Stall bit. If the MCU recognizes the token is wrong, the MCU clears EP0OPR bit and sets this bit. USB generates STALL handshake to current control transfer. MCU write 0 in order to finish STALL.	0
4	R	Set	EP0STED: EP0 Setup End bit. Read Only bit. If control transfer is finished before set the EP0DED bit, USB set this bit. When USB sets this bit, MCU receives interrupt. In this case, USB flushed FIFO, and invalidates FIFO access from MCU. If the FIFO access is validated, this bit is cleared.	0
3	Set/R	Clear	EP0DED: EP0 Data End bit. MCU sets this bit at following conditions. - EP0OPR bit is cleared after takes the last data packet. - EP0OPR bit is cleared and EP0IPR is set in Zero length data phase. - MCU sets EP0IPR bit and this bit (EP0DED) after MCU loads packet data from FIFO.	0
2	Clear/ R	Set	EP0STSTAL: Sent Stall bit. If control transaction is finished by protocol error, USB set this bit. If this bit is set, interrupt is occurred.	0
1	Set/R	Clear	EP0IPR: EP0 In Packet Ready bit. MCU set this bit after writes data into Endpoint0 FIFO. If the data packet is transferred to host successfully, USB clears this bit. If USB clears this bit, interrupt is occurred. Therefore, MCU can keep loading the next data. MCU set EP0IPR and EP0DED in Zero length data phase at the same time.	0
0	R	Set	EP0OPR: EP0 Out Packet Ready bit. Read only. if valid token is written in FIFO, USB set this bit. USB sets this bit, interrupt is occurred. By writing value 1 to EP0OPRC, MCU clears this bit.	0

13.3.12 USB IN Control 1 Register (USBIC1)

Address : 0xF000_102Ch

Bit	R/W		Description	Default Value
	MCU	USB		
31 : 7	R		Reserved	
6	Set	R/Clear	ICCDT: In Control 1 Clear Data Toggle bit. Write Only. If MCU writes 1 to this bit, data toggle bit is cleared.	0
5	R/ Clear	Set	ICSTSTAL: In Control 1 Sent Stall bit. Because MCU sets ICSDSTAL bit, STALL handshake is occurred in the In token. At the time, USB sets this bit. If USB generates STALL handshake, ICIPR bit is cleared. By writing 0, this bit is cleared.	0
4	R/W	R	ICSDSTAL: In Control 1 Send Stall bit. In order to generate STALL handshake to USB, MCU writes 1 to this bit. To finish the STALL, MCU clears this bit.	0
3	R/Set	Clear	ICFFLU: In Control 1 FIFO Flush bit. In order to flush IN FIFO, MCU set this bit. If FIFO is flushed, this bit is cleared by USB. In this circumstance, interrupt is occurred. If a token is processing, USB waits for finish the data transfer. If two packets are loaded into FIFO, the first packet (that will be sent to host) is flushed and the corresponding ICIPR bit is cleared.	0
2			Reserved	0
1	R	Set	ICFNE: In Control 1 FIFO Not Empty bit. This bit represents that FIFO contains at most 1 data packet. 0: No packet inside FIFO. 1: The FIFO holds packets.	0
0	Set / R	Clear	ICIPR: In Control 1 In Packet Ready bit. After write data to FIFO, MCU set this bit. If data packet transfer is success, USB clears this bit. If USB clears this bit, interrupt is occurred, and MCU can load the next packet. During this bit is set, MCU cannot write FIFO. If MCU set ICSDSTAL, this bit cannot be set.	0

13.3.13 USB IN Control 2 Register (USBIC2)

Address : 0xF000_1030h

Bit	R/W		Description	Default Value
	MCU	USB		
31 : 8	R		Reserved	
7	R/W	R	ICASET: In Control 2 Auto Set bit. If this bit is set, MCU set ICIPR bit automatically when MCU writes data as MAXP. In the case of write smaller size data than XAXP, MCU should set ICIPR bit.	0
6			Reserved	0
5	R/W	R	ICMODIN: In Control 2 Mode In bit. With this bit, the direction of Endpoint can be programmable. 1 = In Endpoint 0 = Out Endpoint	1
4 : 0			Reserved	

13.3.14 USB Out Control Register 1 (USBOC1)

Address : 0xF000_1038h

Bit	R/W		Description	Default Value
	MCU	USB		
31 : 8	R		Reserved	
7	R/W	R	OCCDT: Out Control 1 Clear Data Toggle bit. If MCU write 1 to this bit, data toggle sequence bit is reset to DATA0.	0
6	Clear/ R	Set	OCSTSTAL: Out Control 1 Sent Stall bit. When OUT token is finished by the STALL handshake, USB set this bit. If OUT Token sends larger size of data than MAXP, USB generates STALL handshake to host. If MCU writes 0, this bit is cleared.	0
5	W/R	R	OCSDSTAL: Out Control 1 Send Stall bit. MCU writes 1 to this bit in order to generate STALL handshake to USB. In order to finish the STALL status, MCU write 0 into this bit.	0
4	R/W	Clear	OCFFLU: Out Control 1 FIFO Flush bit. MCU writes 1 to this bit in order to flush FIFO and write 0 to stop. Only during OCOPR bit is set, this bit can be set. Data packet that is taken by MCU will be flushed.	0
3	R	R/W	OCERR : Out Control 1 Data Error bit This bit represents that there are errors (bit stuffing or CRC) in received data. This bit is cleared automatically when OCOPR bit is cleared.	0
2	R	R	Reserved	
1	R	R/W	OCFFUL: Out Control 1 FIFO Full bit. This bit represents that FIFO is Full. 0: FIFO is not full. 1: FIFO is full.	0
0	R/ Clear	Set	OCOPR: Out Control 1 Out Packet Ready bit. When data packet is loaded into FIFO, USB set this bit. After MCU reads entire packet, this bit should be cleared by MCU. MCU write 0 to this bit in order to clear.	0

13.3.15 USB OUT Control Register 2 (USBOC2)

Address : 0xF000_103Ch

Bit	R/W		Description	Default Value
	MCU	USB		
31 : 8	R		Reserved	
7	R/W	R	OCACLR: Out Control 2 Auto Clear bit. If this bit is set, whenever MCU reads data from OUT FIFO, OCOPR bit is cleared automatically by USB core.	0
6 : 0			Reserved	0

13.3.16 USB Low Byte Out Write Count Register (USBLOWC)

Address : 0xF000_1040h

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	
7 : 0	R/W	(LBOWC) Low Byte OEP write count register	0x00

13.3.17 USB High Byte Out Write Count Register (USBHBOWC)

Address : 0xF000_1044h

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	
7 : 0	R/W	(HBOWC) High Byte OEP write count register	0x00

13.3.18 EP0 FIFO Data Register (USBEP0)

Address : 0xF000_1048h

Bit	R/W	Description	Default Value
7 : 0	R/W	EP0 FIFO Data Register	0x00

13.3.19 EP1 FIFO Data Register (USBEP1)

Address : 0xF000_104Ch

Bit	R/W	Description	Default Value
31 : 0	R/W	EP1 FIFO Data Register	0x00

13.3.20 EP2 FIFO Data Register (USBEP2)

Address : 0xF000_1050h

Bit	R/W	Description	Default Value
31 : 0	R/W	EP2 FIFO Data Register	0x00

13.3.21 EP3 FIFO Data Register (USBEP3)

Address : 0xF000_1054h

Bit	R/W	Description	Default Value
7 : 0	R/W	EP3 FIFO Data Register	0x00

13.3.22 EP4 FIFO Data Register (USBEP4)

Address : 0xF000_1058h

Bit	R/W	Description	Default Value
7 : 0	R/W	EP4 FIFO Data Register	0x00

14 USB Host Controller (*TBD)

(*Notice. TBD means “To be determined”)

USB 1.1 Host Controller comply with OpenHCI(ver 1.0a).

14.1 Features

- OpenHCI1.0 compatible
- USB 1.1 compatible

14.2 Operational Registers

Table 14-1 USB Host Registers List

Address	***Registers***
A0000000	HcRevision
A0000004	HcControl
A0000008	HcCommandStatus
A000000C	HcInterruptStatus
A0000010	HcInterruptEnable
A0000014	HcInterruptDisable
A0000018	HcHCCA
A000001C	HcPeriodCurrentED
A0000020	HcControlHeadED
A0000024	HcControlCurrentED
A0000028	HcBulkHeadED
A000002C	HcBulkCurrentED
A0000030	HcDoneHead
A0000034	HcFmInterval
A0000038	HcFmRemaining
A000003C	HcFmNumber
A0000040	HcPeriodicStart
A0000044	HcLSThreshold
A0000048	HcRhDescriptorA
A000004C	HcRhDescriptorB
A0000050	HcRhStatus
A0000054	Reserved.
A0000058	HcRhPortStatus[1]

15 AHB DMA

15.1 Features

- Compatibility with AMBA AHB Specification
- Provides 4 channels. Each channels supports DMA.
- 16-port DMA Request.
  - DMAC provides 16-port DMA Request signal for Peripherals.
- Provides Single Request and Burst Request.
  - DMA request that provides to peripherals supports both Single Request and Burst Request.
- 4 types of DMA communication
  - DMA provides memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral communications.
- Provides Scatter and Gather by using Auto Reload functionality.
- Provides Scatter and Gather by using Linked list
- Priority of the DMA channel is fixed by hardware. Channel 0 has the highest priority and channel 7 has the lowest priority.
- Provides Multi-Layer AHB Bus by embedding 2 AHB Master.
- Provides Programmable Burst Size. In order to achieve higher efficiency of DAM transmit, user can configure Burst Size. The Burst Size is generally configured as half size of that of FIFO which is embedded in Peripheral.
- Each channel has 4 Word FIFO.
- Each channel has separated DMA Error Interrupt and DMA Terminal Count Interrupt.
- Supports Interrupt Enable.
  - DMA has an enable bit for both DMA Error Interrupt and DMA Terminal Count Interrupt.

15.2 Block Description

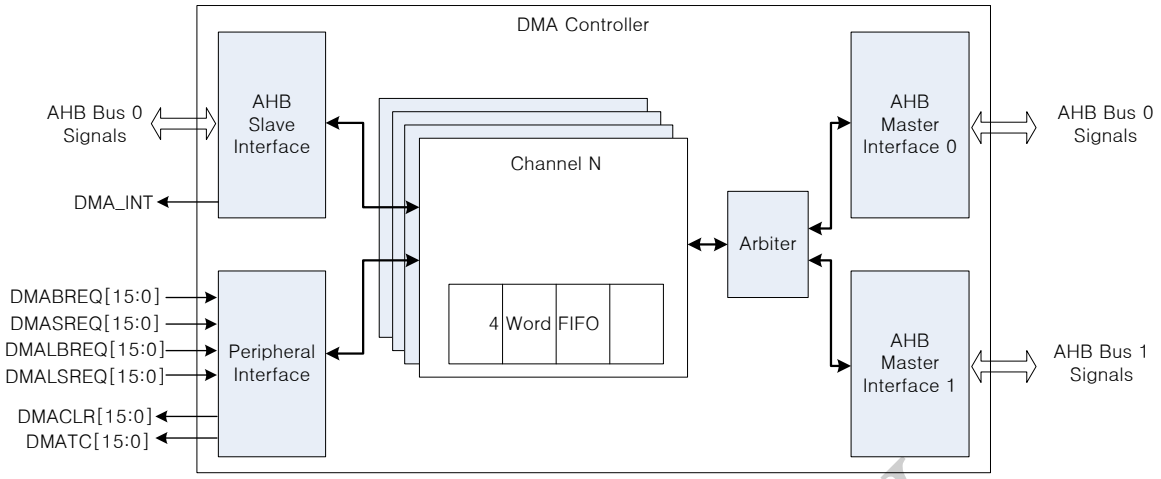


Figure 15-1 DMA Block Diagram

DMA has 8-channel. Each channel controls data flow that one-direction transfers from Source Peripheral to Destination Peripheral and contains 4x4 byte FIFO.

AHB Master Interface is responsible for data transmit from/to AHB Bus after receive data transfer requests from each channel. Inside the DMA Controller, because there are 2 AHB Master Interface, the DMA Controller can connect to other bus interface. Due to that reason, in spite of both Source Peripheral and Destination Peripheral connect to other bus, they can transfer data.

The Arbiter transmits data to AHB Master Interface0 or AHB Master Interface1 according to priority of data transfer request. It is determined by data address which AHB Master Interface should be use.

AHB Slave Interface is responsible for configures registers of each channel and requests interrupt.

Peripheral Interface receives DMA Request signal from Peripherals and send a signal to the corresponding channel according to Peripheral Selection bit. The Peripheral Interface can receive maximum 16 DMA Request signals. The channel can receive 2 DMA request signals Source DMA Request signal and Destination DMA Request signal.

15.3 Function Description

15.3.1 DMA Operation

15.3.1.1 Transfer Hierarchy

DMA transfer has 3-layer hierarchy as figure 9-2.

The highest layer is called DMA Transfer. DMA Transfer indicates total size of data that is transferred by DMA. The size of transmit is determined by Transfer size of Control register.

The second layer is called Burst Transaction. Amount of data that is transferred from Burst Transaction is determined by Burst Size of Control register. Generally, the size is set to FIFO size of peripherals. Because the peripherals cannot transfer all of data at one time, the peripherals separates data in the unit of FIFO size and sends it.

** The burst size of control register is not AMBA Burst Transfer's burst size.

The lowest layer is called AMBA Burst Transfer. The Burst Transaction is divided into AMBA Burst Transfer unit. In this layer, data transfer is controller by hardware not user.

User can configures smaller Transfer Size than Burst Size. In that case, the Burst Transaction sends data with configured Transfer size.

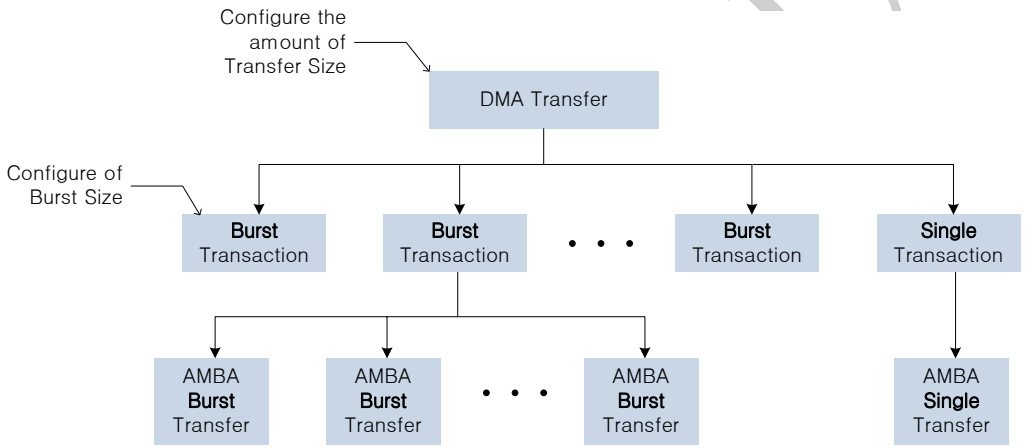


Figure 15-2 DMA Transfer hierarchy

15.3.1.2 Transfer type

User should specify that Transfer type in DMA configuration. The transfer type is one of following 4 types.

1. Memory to Memory
2. Memory to Peripheral
3. Peripheral to Memory
4. Source Peripheral to Destination Peripheral

Memory to Memory type indicates that a source address is Memory and also a destination address is memory.
Memory to Peripheral type indicates that a source address is Memory and Destination address is Peripheral. In order words, with this type, DMA transfers data from Memory to Peripheral buffer.

The reason that user should specify the Transfer type is informing to DMA that whether handshake process is necessary or not. DMA uses handshake method when transfers data between peripherals memory To transfer data between peripherals not memory, the peripherals needs preparation and time. Also, the size of transmit is limited. With the handshake method, DMA Controller transfers data only when the data is ready. However, in the case of the peripheral is memory, it is not necessary. that handshake process, because Memory can be accessed anytime. Therefore, user should specify the transfer type and inform to DMA Controller that data transmit is handshake method or not.

15.3.1.3 Flow Controller

Flow Controller is a module that determines DMA Transfer size. Flow Controller is DMA Controller or one of Peripherals. If DMA Controller is Flow Controller, then the DMA data transfer size is determined as configured Transfer Size.

Also, a peripheral can be Flow Controller. In this case, DMA Controller transfers data according to request signal of Peripheral and ignores configured Transfer size. In order to finish DMA Transmit, when Flow Controller requires the last data, DMA Controller sends Last Request. Once the DMA Controller receives Last Request, the DAM transmit is finished after sending the last data.

15.3.2 Linked List Operation

15.3.2.1 LLI

LLI (Linked List Item) is a data structure that contains basic information to DMA transmits. The contents of LLI are Source Address, Destination Address, Next LLI Address, and Control information. Linked List Operation is that reading first LLI and updates internal registers. After that, the operation does DMA Transfer When the DMA transfer is finished, the operation reads the next LLI according to the next LLI address. Following figure 9-3 depicts LLI structure.

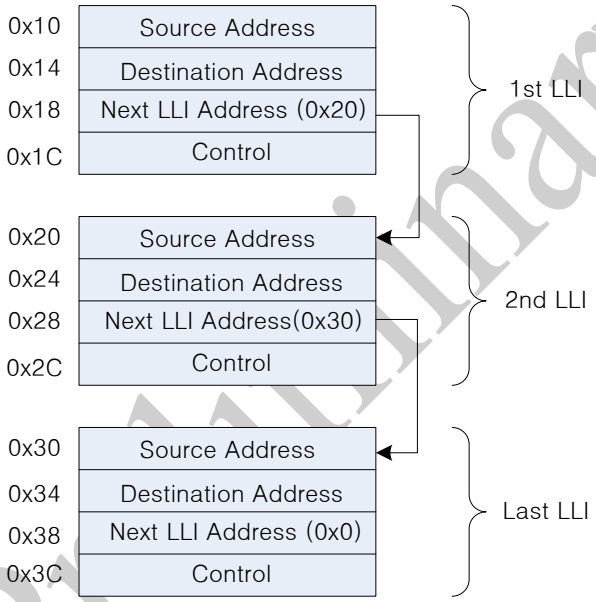


Figure 15-3 Linked list

The next LLI address of the last LLI is reserved as 0. If DMA Controller confirms the Next LLI address is 0, the DMAC can know the LLI is the last. Therefore, if an address of LLI is 0, the LLI operation cannot be executed.

15.3.2.2 Multi Block Transfer

Transfers data that is described as LLI structure is called Multi Block Transfer. In order words, LLI data is defined as Block. The number of LLI refers to the number of Block. Also, the size of Block is defined as Control register's Transfer Size. The following figure 9-4 shows hierarchical view of Multi Block Transfer.

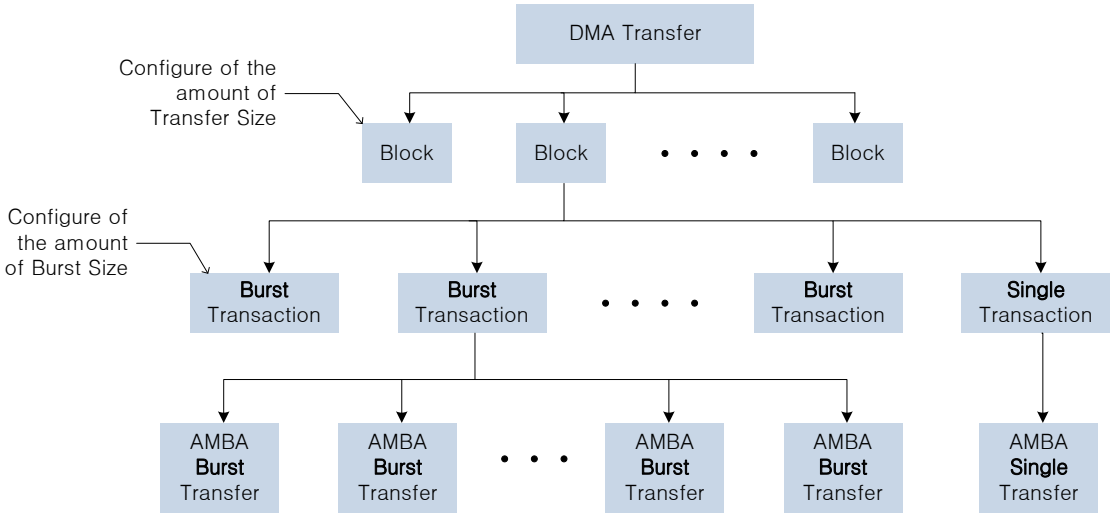


Figure 15-4 Multi Block Transfer

15.3.2.3 Scatter & Gather with Liked list

Scatter indicates spread data by DMA Transfer and Gather indicates that putting together the separated data. User can the Scatter and Gather operations by using LLI.

The following figure 9-5 shows an example for Gather operation by using LLI. In the figure, data is depicted as rectangle and the data is copied into peripheral.

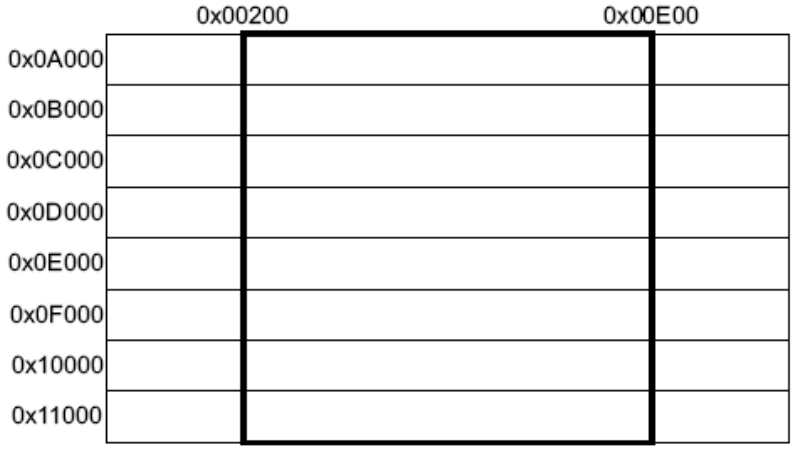


Figure 15-5 Gathering by using LLI

LLI starts from address 0x20000

The contents of the first LLI

- Source Address: 0x0A200
- Destination Address: Peripheral Address
- Source and Destination transfer width: 8bit
- Source and Destination burst Size: 16 burst
- Transfer Size: 3072 byte, 0xC00
- Next LLI Address: 0x20010

The contents of the second LLI
- Source Address: 0x0B200
- Destination Address: Peripheral Address
- Source and Destination transfer width: 8bit
- Source and Destination burst Size: 16 burst
- Transfer Size: 3072 byte, 0xC00
- Next LLI Address: 0x20020

The Contents of the last LLI
- Source Address: 0x11200
- Destination Address: Peripheral Address
- Source and Destination transfer width: 8bit
- Source and Destination burst Size: 16 burst
- Transfer Size: 3072 byte, 0xC00
- Next LLI Address: 0x0

15.3.3 Auto Reload Operation

The basic operation of Auto Reload Operation is when DMA Transfer is finished; reload Control register value to repeat DMA Transfer.
The number of repeat count is determined by Auto Reload Count Register. The value of Auto Reload Count decreases by 1 when Auto Reload is occurred. If the value is 0, the Auto Reload Operation is stopped. The Auto Reload Operation is not necessary to mode configuration additionally. When finish DMA Transfer, if the value of Auto Reload Count Register is not 0, the Auto Reload Operation does not operate.

- **Transfer Hierarchy**

  Auto Reload Operation is categorized in Multi Block Transfer like as Linked List Operation. The number of Block is Auto Reload Count + 1, and the size of data transferred is set to Transfer Size.

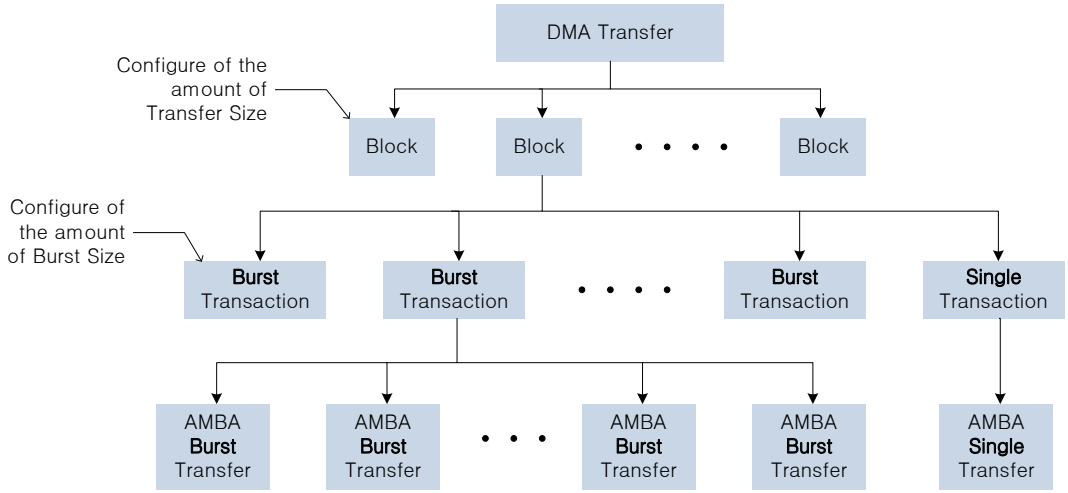


Figure 15-6 Auto Reload Operation Transfer Hierarchy

15.3.3.1 Scatter with Auto reload

The following figure 9-7 shows an example for Scatter with Auto Reload Operation. Whenever finishing Block data transfer, Destination Scatter Address indicates uniform size of space between Destination Blocks′ start address. User can separate between Blocks and can implement Scatter operation by using the Destination Block Address Register.

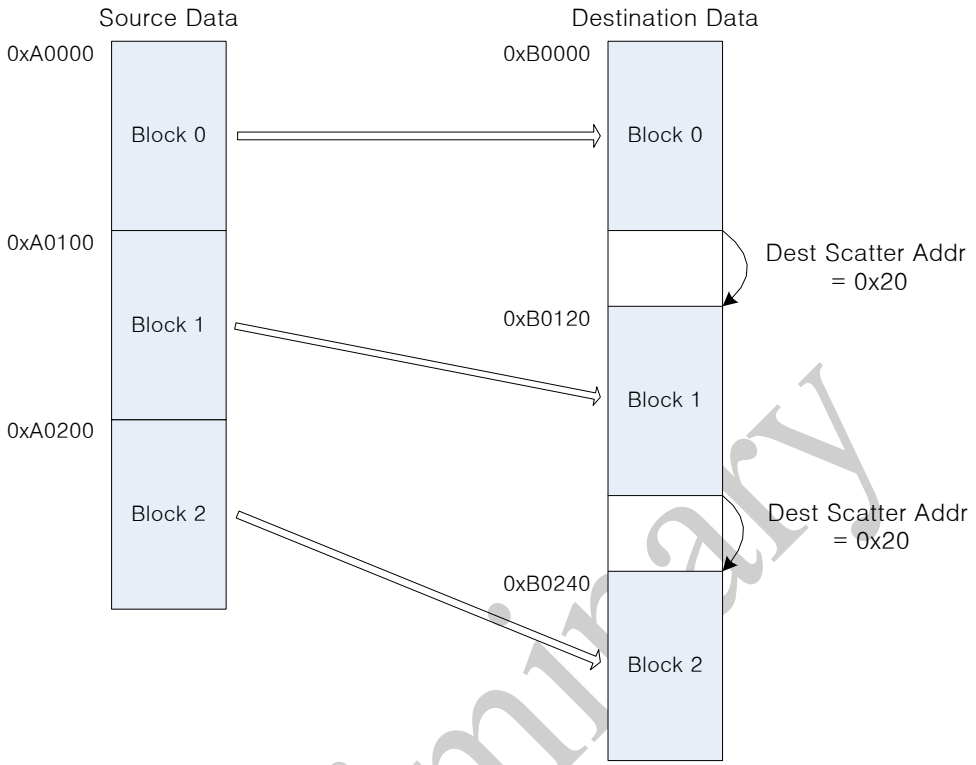


Figure 15-7 Scatter with Auto Reload Operation

Register Configuration

- Source Address: 0xA0000
- Destination Address: 0xB0000
- Source and Destination transfer width: 32bit
- Source and Destination burst Size: 4 burst
- Transfer Size: 0x40
- Auto Reload Count: 2
- Destination scatter Address: 0x20

15.3.3.2 Gather with Auto reload

The following figure 9-8 shows an example for Gather with Auto Reload Operation. Whenever finishing Block data transfer, Source Gather Address indicates uniform size of space between Source Blocks' start address. User can separate between Blocks and can implement Gather operation by using the Source Block Address Register.

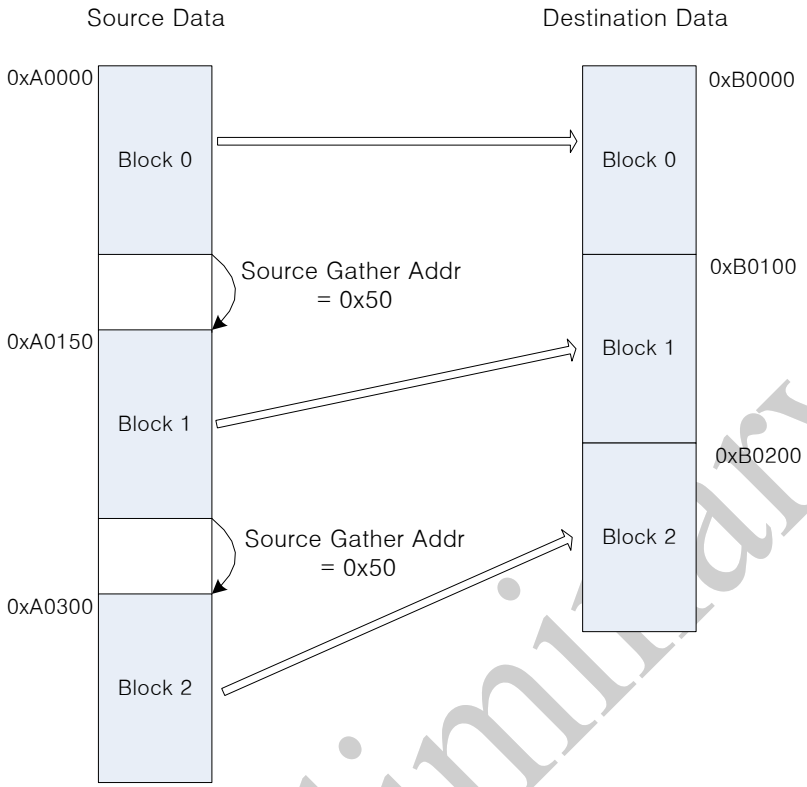


Figure 15-8 Gather with Auto Reload Operation

Register Configuration

- Source Address: 0xA0000
- Destination Address: 0xB0000
- Source and Destination transfer width: 32bit
- Source and Destination burst Size: 4 burst
- Transfer Size: 0x40
- Auto Reload Count: 2
- Source gather Address: 0x50

15.3.4 Peripheral Interface

15.3.4.1 Hand Shake Signals

DMA Request signal and DMA Clear signal is used for Handshake DMA data transfer between Peripherals not memory.

Four DMA Request signals are used when peripheral requests data transfer to DMA Controller (Refer to Figure 9-9). Peripheral selects one signal of the 4, and requests. It is not allow to select multiple signal at the same time.

DMA Clear signal is a response of DMA Request. DMA Controller sends the signal to Peripheral.

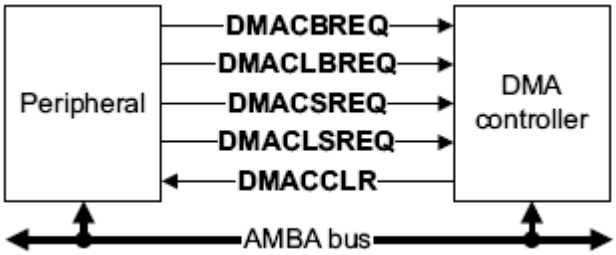


Figure 15-9 DMA Handshake Signals

- DMABREQ
  - Burst Request signal. If the signal is activated, DMA Data Transfer becomes Burst Transaction by DMA Controller and the size of data is determined by Burst Size.
- DMASREQ
  - Single Request signal. If the signal is activated, DMA Data Transfer becomes Single Transaction.
- DMALBREQ
  - Last Burst Request. When peripheral is Flow Controller, this signal is used for informing that data is the last DMA Burst Request. If DMALBREQ is activated, the last Burst Transaction is operated and DMA Transfer is finished.
- DMALSREQ
  - Last Single Request. When peripheral is Flow Controller, this signal is used for informing that data is the last DMA Single Request. If DMALBREQ is activated, the last Single Transaction is operated and DMA Transfer is finished.
- DMACLR
  - DMA Clear signal. With this signal, all of the Requests from peripheral are inactivated.

15.3.4.2 Time diagram of DMA Request

If peripheral send request to DMA Controller, the DMA Controller programed transfer data amount of Burst Size, and then send DMA Clear signal. At that time, when all of data transfer is finished, DMATC (DMA Terminal Count) signal is activated. With the signal, peripheral can check whether the DMA data transfer is finished or not.

When peripheral receives DMA Clean signal (DMACLR), DMA Request signal is inactivated. If peripheral inactivates DMA Request before receives DMA Clear signal, it can be a problem. Also, peripheral tries to send Next DMA Request signal, it is possible only when the current DMA Clear signal is inactivated.

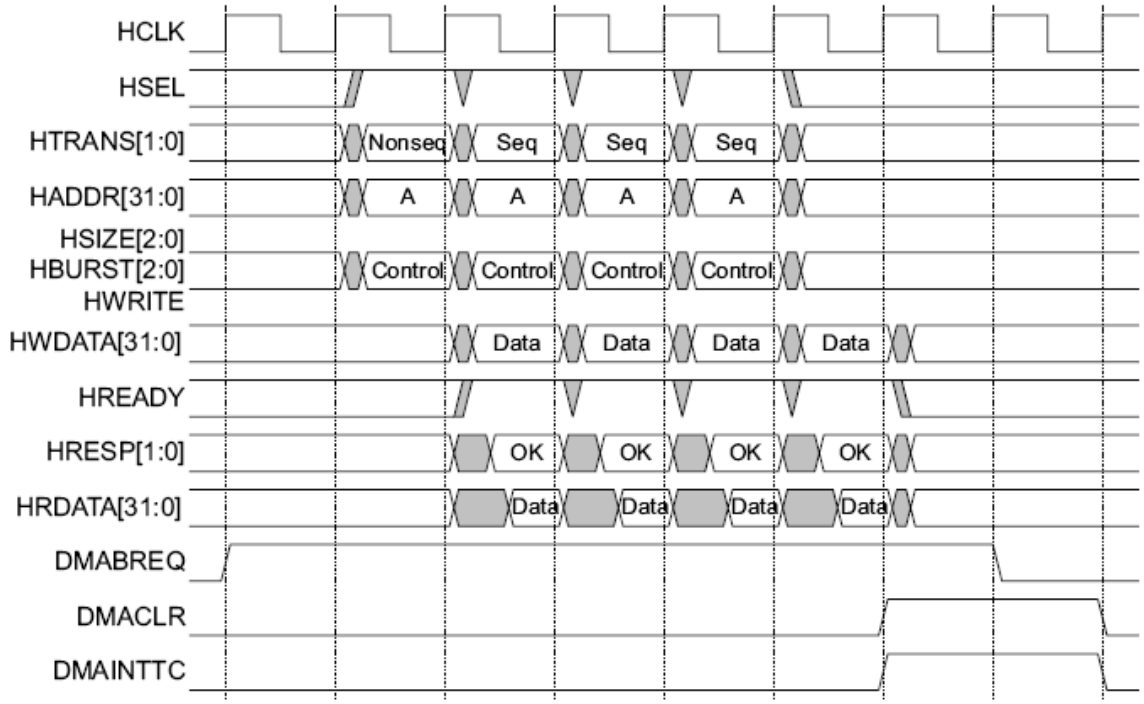


Figure 15-10 Time Diagram of DMA Request

15.4 Register Description

15.4.1 DMA Interrupt Status (DMAIntStatus)

Address: 0xF000_1800

Bit	*R/W*	*Description*	*Default Value*
31 : 8	R	Reserved	
7 : 0	R	Interrupt Status of Channel This register indicates interrupt request status from each channel. ex) If bit 0 is set, interrupt is occurred from channel 0. If bit 1 is set, interrupt is occurred from channel 1. Because there are 2 types of interrupt, user should check interrupt type by reading DMATCIS and DMATCIC registers.	0

15.4.2 DMA Terminal Count Interrupt Status (DMATCIntStatus)

Address: 0xF000_1804

Bit	*R/W*	*Description*	*Default Value*
31 : 8	R	Reserved	
7 : 0	R	Terminal Count Interrupt Status of Channel This register indicates whether Terminal Count Interrupt is occurred or not from each channel.	0

15.4.3 DMA Terminal Count Interrupt Clear (DMATCIntClr)

Address: 0xF000_1808

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	
7 : 0	W	Terminal Count Interrupt Clear Each bit of this register has responsible for clear Terminal count interrupt. If the bit is set, a correspond channel's interrupt is cleared.	0

15.4.4 DMA Error Interrupt Status (DMAErrorIntStatus)

Address: 0xF000_180C

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	
7 : 0	R	Error Interrupt Status of Channel The register indicated that whether the DMA Transfer error interrupt is occurred or not.	0

15.4.5 DMA Error Interrupt Clear (DMAErrorIntClr)

Address: 0xF000_1810

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	
7 : 0	W	Error Interrupt Clear Each bit has responsible for clearing DMA Transfer error interrupt. If the bit is set, the corresponding channel's interrupt is cleared.	0

15.4.6 DMA Block Interrupt Status (DMABlockIntStatus)

Address: 0xF000_1814

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	
7 : 0	R	Block Interrupt Status of Channel With this register, user can know whether DMA Block interrupt is occurred or not.	0

15.4.7 DMA Block Interrupt Clear (DMABlockIntClr)

Address: 0xF000_1818

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	
7 : 0	W	Block Interrupt Clear Each bit has responsible for clearing DMA Block interrupt. If the bit is set, the corresponding channel's interrupt is cleared.	0

15.4.8 DMA Raw Terminal Count Interrupt Status (DMARawTCIntStatus)

Address: 0xF000_181C

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	
7 : 0	R	Raw Terminal Count Interrupt Status of Channel This register informs that each channel's Terminal Count Interrupt is occurred when the channel is disabled by interrupt Enable bit.	0

15.4.9 DMA Raw Error Interrupt Status (DMARawErrorIntStatus)

Address: 0xF000_1820

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	
7 : 0	R	Error Interrupt Status of Channel This register informs that each channel's Error Interrupt is occurred.	0

15.4.10 DMA Enabled Channel Status (DMAEnbldChn)

Address: 0xF000_1824

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	
7 : 0	R	Enabled Channel Status Each bit informs that DAM is Enabled or Disabled.	0

15.4.11 DMA Software Burst Request (DMASoftBReq)

Address: 0xF000_1828

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	
15 : 0	RW	Software Burst Request The register generates DMA Burst Request signal in software. If user write 1 to correspond bit, DMA Burst Request signal is sent and Clear is automatically operates	0

15.4.12 DMA Software Single Request (DMASoftSReq)

Address: 0xF000_182C

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	
15 : 0	RW	Software Single Request The register generates DMA Single Request signal in software. If user writes 1 to corresponding bit, DMA Single Request signal is sent and Clear is automatically operates.	0

15.4.13 DMA Software Last Burst Request (DMASoftLBReq)

Address: 0xF000_1830

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	
15 : 0	RW	Software Last Burst Request The register generates DMA Last Burst Request signal in software. If user writes 1 to correspond bit, DMA Last Burst Request signal is sent and Clear is automatically operates.	0

15.4.14 DMA Software Last Single Request (DMASoftLSReq)

Address: 0xF000_1834

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	
15 : 0	RW	Software Last Single Request The register generates DMA Last Single Request signal in software. If user writes 1 to correspoing bit, DMA Last Single Request signal is sent and Clear is automatically operates.	0

15.4.15 Channel Source Address Register (ChnSrcAddr)

Address: 0xF000_1900 / 0xF000_1920 / 0xF000_1940 / 0xF000_1960

Bit	R/W	Description	Default Value
31 : 0	RW	Source Address This register sets Source Address of each channel. The configured address value should fit alignment according to Source transfer width. Source Address automatically increases as data transfer. Due to this reason, this register should hold data address to send always. However, the source address value during a channel operation (Data transfer) is insignificant. Because the channel keeps operating data transfer, even though program reads the source address. But, after finishing the channel's data transmit, if user checks the register, user can confirm that all of data is read or not.	0

15.4.16 Channel Destination Address Register (ChnDstAddr)

Address: 0xF000_1904 / 0xF000_1924 / 0xF000_1944 / 0xF000_1964

Bit	R/W	Description	Default Value
31 : 0	RW	Destination Address This register sets Destination Address of each channel. The configured address value should fit alignment according to Destination transfer width. Destination Address automatically increases as data transfer. Due to this reason, this register should hold data address to send always. However, the destination address value during a channel operation (Data transfer) is insignificant. Because the channel keeps operating data transfer, even though program reads the source address. But, after finishing the channel's data transmit, if user checks the register, user can confirm that all of data is read or not.	0

15.4.17 Channel Linked List Item Register (ChnLLI)

Address: 0xF000_1908 / 0xF000_1928 / 0xF000_1948 / 0xF000_1968

Bit	R/W	Description	Default Value
31 : 2	RW	Linked List Item Address This register specifies start address of Linked List Item of each channel. If the value of the register is not 0x0 and the channel is enabled, DMA Controller loads Linked List Item from the start address. After that, DMA Controller updates internal registers and executes Linked List Operation. With the default value (0x0) of the register DMA Controller does not executes Linked List Operation.	0
1 : 0	R	Reserved	0

15.4.18 Channel Control Register (ChnCntl)

Address: 0xF000_190C / 0xF000_192C / 0xF000_194C / 0xF000_196C

Bit	R/W	Description	Default Value
31 : 30	R	Reserved	-
29	RW	Destination Increment If set this bit, destination address is automatically increased according to data transfer.	0
28	RW	Source Increment If set this bit, source address is automatically increased according to data transfer.	0
26 : 24	RW	Destination transfer width 000 : 8bit 100 : Reserved 001 : 16bit 101 : Reserved 010 : 32bit 110 : Reserved 011 : Reserved 111 : Reserved This bit configures data width of destination. It can be set differently from source transfer width. If the destination transfer width is smaller than source transfer width, user should carefully configure Transfer size. (Refer to Program Consideration)	0
23	R	Reserved	
22 : 20	RW	Source transfer width 000 : 8bit 100 : Reserved 001 : 16bit 101 : Reserved 010 : 32bit 110 : Reserved 011 : Reserved 111 : Reserved This bit configures data width of source.	0
19	R	Reserved	
18 : 16	RW	Destination burst size 000 : 1 100 : 32 001 : 4 101 : 64 010 : 8 110 : 128 011 : 16 111 : 256 This bits configures Burst Transaction Size of destination peripheral. It is almost same as AHB Burst Size, but it is upper level transaction that includes the AHB Burst Size. (Refer to Transfer Hierarchy). In the case of the destination is memory, the register works same manner.	0
15	R	Reserved	
14 : 12	RW	Source burst size 000 : 1 100 : 32 001 : 4 101 : 64 010 : 8 110 : 128 011 : 16 111 : 256	0

		This bits configures Burst Transaction Size of source peripheral. It is almost same as AHB Burst Size, but it is upper level transaction that includes the AHB Burst Size. (Refer to Transfer Hierarchy). In the case of the source is memory, the register works same manner.	
11 : 0	RW	Transfer Size When DMA Controller is Flow Controller, this register indicates the total size of transferred data from DMA channel. The unit of transfer is not Byte but Source Transfer Width. In order words, the total size of data transfer is calculated as (Transfer size) x (source transfer width) This value is decreased as 1 when transfers data. Once the value is 0, DMA Transfer is finished. Therefore, user can know remain data size to transfer if user reads the value. If DMA Controller is not Flow Controller, the value is ignored but the value should be 0 in Program.	000

15.4.19 Channel Configuration Register (ChnCfg)

Address: 0xF000_1910 / 0xF000_1930 / 0xF000_1950 / 0xF000_1970

Bit	*R/W*	*Description*	*Default Value*
31 : 22	R	Reserved	0
21	RO	FIFO Active 0: FIFO is empty 1 : FIFO has data	-
20	RW	Halt 0 : enable DMA request 1 : ignore DMA request. User can disable DMA channel by using this bit and clears out FIFO	0
19	RW	Lock If this bit is set, Locked transfer is operated.	0
18	RW	Block Interrupt Enable Interrupt Enable bit when Block transfer is finished with Multi Block Transfer. If Block Interrupt is occurred, DMA does not transfer Next Block until the Block Interrupt is cleared.	
17	RW	Terminal count interrupt Enable Enable bit for DMA Transfer finish interrupt.	0
16	RW	Interrupt error Enable Enable bit for DMA Error Interrupt.	0
15	R	Reserved	0
14 : 12	RW	Flow Control Value | Transfer type | Flow controller 000 | Memory-to-Memory (Default) | DMA 001 | Memory-to-Peripheral | DMA 010 | Peripheral-to-Memory | DMA 011 | Source peripheral-to-destination peripheral | DMA 100 | Source peripheral-to-destination peripheral | Dst. Peri. 101 | Memory-to-Peripheral | Peripheral 110 | Peripheral-to-Memory | Peripheral 111 | Source peripheral-to-Destination peripheral | Src. Peri. This bit determines both Transfer type and Flow Controller.	
11 : 8	RW	Destination Peripheral This bit selects one of the 16 DMA Requests. 0000: NAND Flash TX 0001: SDHC 0010: Reserved 0011: Reserved 0100: USB Device Bulk In 0101: Mixer Play CH0 0110: Mixer Play CH1 0111: Mixer Play CH2 1000: Mixer Play CH3 1001: Reserved … 1110: Reserved 1111: Reserved	0
7 : 4	RW	Source Peripheral This bit selects one of the 16 DMA Requests. 0000: Reserved 0001: SDHC 0010: NAND Flash RX 0011: USB Device Bulk Out 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Mixer Record 1010: ADC …	0

		1110: Reserved 1111: Reserved	
3 : 1	R	Reserved	0
0	RW	Channel Enable Channel can be activated by this bit. In order to do DMA Transfer, user sets this bit. If the bit is set to 1, DMA Transfer is started with configuration. If the DMA Transfer is finished, this bit is automatically cleared. Auto Clear conditions are following. Finish DMA Transfer Finish Linked List Operation Finish Auto Reload Operation Finished by Error User can finish the activated channel manually by clearing the Enable bit. However, in this case, all of channel FIFO data is removed.	0

15.4.20 Channel Source Gather Address Register (ChnSrcGaAddr)

Address: 0xF000_1914 / 0xF000_1934 / 0xF000_1954 / 0xF000_1974

Bit	*R/W*	*Description*	*Default Value*
31 : 16	R	Reserved	-
16	RW	Auto Reload Source Address If this bit is set, Source Address is reloaded with initially configured source address when Auto Reload.	
15 : 0	RW	Source Gather Address When Auto Reload is operated, the Source Address is added with Source Gather Address.	0

15.4.21 Channel Destination Scatter Address Register (ChnDstScaAddr)

Address: 0xF000_1918 / 0xF000_1938 / 0xF000_1958 / 0xF000_1978

Bit	*R/W*	*Description*	*Default Value*
31 : 16	R	Reserved	-
16	RW	Auto Reload Destination Address If this bit is set, Destination Address is reloaded with initially configured source address when Auto Reload.	
15 : 0	RW	Destination Scatter Address When Auto Reload is operated, the Destination Address is added with Destination Scatter Address.	0

15.4.22 Channel Auto Reload Count Register (ChnAutoReloadCnt)

Address: 0xF000_191C / 0xF000_193C / 0xF000_195C / 0xF000_197C

Bit	*R/W*	*Description*	*Default Value*
31 : 22	R	Reserved	-
21	RW	Uncountable Auto Reload If this bit is set, Auto Reload is operated regardless of Auto Reload Count.	
20 : 0	RW	Auto Reload Count User can specify Auto Reload Count to this bits and can repeat DMA Transfer. The Auto Reload count is decreased when Block transfer is finished (Transfer Size becomes 0). If the value becomes 0, Auto Reload Operation is finished.	0

15.5 Program Guide

15.5.1 Summary of Register

Name	Address	Type	Description
DMAIntStatus	0x000	R	DMA Interrupt Status
DMATCIntStatus	0x004	R	DMA Terminal Count Interrupt Status
DMATCIntClr	0x008	W	DMA Terminal Count Interrupt Clear
DMAErrorIntStatus	0x00C	R	DMA Error Interrupt Status
DMAErrorIntClr	0x010	W	DMA Error Interrupt Clear
DMABlockIntStatus	0x014	R	DMA Block Interrupt Status
DMABlockIntClr	0x018	W	DMA Block Interrupt Clear
DMARawTCIntStatus	0x01C	R	DMA Raw Terminal Count Interrupt Status
DMARawErrorIntStatus	0x020	W	DMA Raw Error Interrupt Status
DMAEnbldChns	0x024	R	DMA Enabled Channels
DMASoftBReq	0x028	RW	DMA Software Burst Request
DMASoftSReq	0x02C	RW	DMA Software Single Request
DMASoftLBReq	0x030	RW	DMA Software Last Burst Request
DMASoftLSReq	0x034	RW	DMA Software Last Single Request
ChnSrcAddr	0x100	RW	Channel Source Address
ChnDestAddr	0x104	RW	Channel Destination Address
ChnLLI	0x108	RW	Channel Linked List Item
ChnCntl	0x10C	RW	Channel Control
ChnCfg	0x110	RW	Channel Configuration
ChnSrcGaAddr	0x114	RW	Channel Source Gather Address
ChnDestScatAddr	0x118	RW	Channel Destination Scatter Address
ChnAutoReloadCnt	0x11C	RW	Channel Auto Reload Count

15.5.2 Programming Sequence

- DMA Operation (Memory to Memory)

1. Choose a channel to transfer
2. Configures Source Address of the channel (ChnSrcAddr Register)
3. Configures Destination Address of the channel (ChnDstAddr Register)
4. Configures Transfer Width of source and destination (ChnCntl Register)
5. Configures Burst Size of source and destination (ChnCntl Register)
6. Configures Transfer Size (DMA Transfer size) (ChnCntl Register)
7. Enables the Channel (ChnCfg Register)
8. Check the DMA Transfer is finished (DMAEnbldChns Register)
9. Finish

- DMA Operation (Memory to Peripheral)

1. Choose a channel to transfer
2. Configures Source Address of the channel (ChnSrcAddr Register)
3. Configures Destination Address of the channel (ChnDstAddr Register)
4. Configures Transfer Width of source and destination (ChnCntl Register)
5. Configures Burst Size of source and destination (ChnCntl Register)
6. Configures Transfer Size (DMA Transfer size) (ChnCntl Register)
7. Configures Transfer Type (ChnCfg Register)
8. Enables the Channel (ChnCfg Register)
9. Check the DMA Transfer is finished (DMAEnbldChns Register)
10. Finish

- Linked List Operation (Memory to Memory)

1. Assumes that the Linked List Item is already prepared.
2. Choose a channel to operate
3. Configures the first LLI address (ChnLLI Register)
4. Enables the channel (ChnCgf Register)
5. Checks the operation is finished (DMAEnbldChns Register)
6. Finish

- Auto Reload Operation Program (Memory to Memory)

1. Choose a channel to operate
2. Configures Source Address of the channel (ChnSrcAddr Register)
3. Configures Destination Address of the channel (ChnDstAddr Register)
4. Configures Transfer Width of source and Destination (ChnCntl Register)
5. Configures Burst Size of source and destination (ChnCntl Register)
6. Configures Transfer Size (DMA Transfer size) (ChnCntl Register)
7. Specifies Auto Reload Size (ChnAutoReloadCnt Register)
8. Enables the Channel (ChnCfg Register)
9. Check the DMA Transfer is finished (DMAEnbldChns Register)
10. Finish

15.5.3 Program Consideration

User program should consider following restrictions.

1. User should not change the channel's register value after the channel is enabled. Because DMA Transfer is operated after the channel is enabled, modifying register value may induce problem. Due to that reason, user should check whether the channel is enabled or disabled to modify register value.

2. DMA Transfer size is set to times of Destination transfer width if source transfer width is smaller than destination transfer width. DMA Transfer size is calculated with the size of read data in source (Source width x Transfer size). If the DMA Transfer size does not match with Destination width x N, the size of written data in destination is smaller or larger.

3. Linked List Item does not allocate in address 0x0.

16 AXI DMA

16.1 Features

- Supports 2 channel
- Supports single transfer and burst transfers
- Supports only memory to memory transfer
- Supports Scatter and gather function
- Supports Linked list transfer
- Each channel supports 4 word FIFO

16.2 Block Description

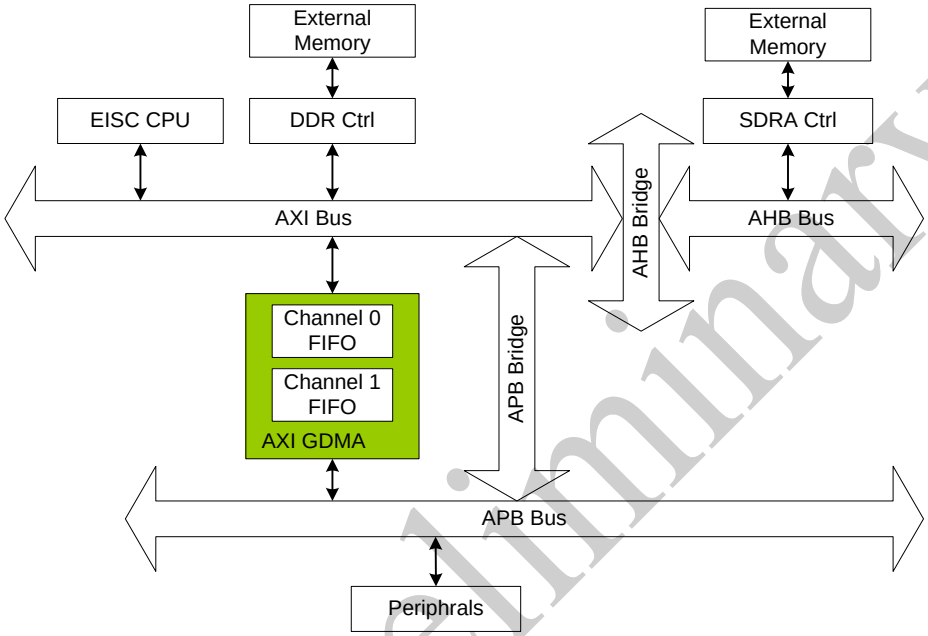


Figure 16-1 AXI DMA Block Diagram

Each DMA Channel has the equal priority. so the earlier request between channels wins the ownership of the bus interface. If equal priority requests occur, then the lower-numbered channel is granted.

DAMC consists of one axi master interface and one apb slave interface
Maximum AXI data width is 32-bit wide.
The address of source or destination is programmed as incremental or fixed.
The burst transfer size is fixed as four.
It supports 8-, 16- and 32-bit transfers.

- Unaligned data is not supported

- Addressing
  - Source address and destination address must be aligned to 32 bits.

16.3 Function Description

DMA request
DMA transfers are not enabled by the hardware request. DMA block transfers is initiated by the software.

DMA channel priority
Each channel has the same priority. Although each channel is enabled at the same time,
the transfer service is granted the channel which source request is earlier other than.
If equal priority request occur, then the lower-numbered channel is granted.

Internal FIFO
4 Word fifo depths per channel. Burst transfer size is four.

Data width
8-, 16- 32-bit data width

Address Generation
Programmable source and destination addresses
Address increment, or no change
Assumed to be aligned to 4KB boundary during burst transfers

Multi-Block transfer (Multi-DMA transfer)
Once the channel is enabled, the transfer proceeds, that transfer is called DMA transfer or Block transfer. The block transfers are broken into the bursts and single transfer.
To enable multiple DMA transfer . uses auto-reload configuration or Linked-list configuration.

Scatter/Gather
Once the DMA transfer has completed, and it can automatically proceeds the next transfers. To enable multiple DMA transfer uses auto-reload configuration or Linked-list configuration.
In this configuration, Scatter/Gather is available.

Auto-Reload Transfer

At the end of each block, DMAC automatically proceeds to next block.
During auto-reloading, at the completion of each block, source address is automatically incremented by the amount of the offset. This processes Gather operation.
During auto-reloading, at the completion of each block, destination address is automatically incremented by the amount of the offset. This processes Scatter operation.

Linked-list Transfer

Multi-block transfers are achieved by Linked-list Transfer.

In this case, the DMAC registers is not reprogrammed by software, they are fetched the descriptor for that block form system memory. This mitigates any workload of processor.

Each Linked-list entry contains the correspond block descriptors.

Address	
0x00	Source Address Register
0x04	Destinaion Address Register
0x08	Next Pointer Register
0x0C	Control 0 Register

Figure 16-2 Descriptor structure

Linked list accesses are always 32-bit accesses. Channel registers prior to the start of each block are reprogramed by fetching the block descriptor for that block form system memory.

To set up block chaining, program a sequence of Linked list in system memory.
1. Next Pointer Register written as the address of the first Descriptor .
2. Enabled by setting Linked-List enable bit in the source/destination Control 0 Register
3. fetching the block descriptor for that block from system memory, then DMA transfer proceeds.

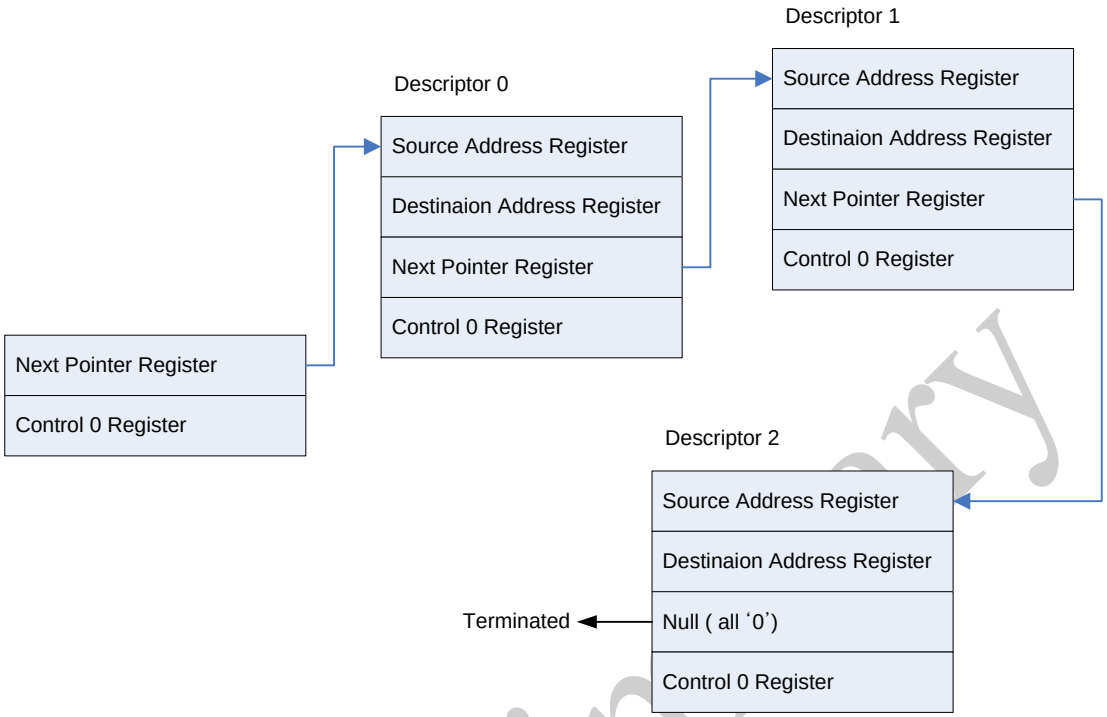


Figure 16-3 Behavior of Descriptor

If the next point register of the last block descriptor in memory is zero. then the DMA transfer is terminated.

Interrupt
The block-complete interrupt is generated at the completion of the block transfer.
To clear interrupt, a write to the corresponding interrupt clear registers

16.4 Register Description

16.4.1 Channel Enable Register

Address: 0xF400_2C00

Bit	*R/W*	*Description*	*Default value*
31 : 2	R	Reserved	
1	R/W	Enables/Disables Channel 1. 0 : Disable Channel 1 1 : Enable Channel 1 Automatically cleared by hardware at the completion of transfer.	0
0	R/W	Enables/Disables Channel 0. 0 : Disable Channel 0 1 : Enable Channel 0 Automatically cleared by hardware at the completion of transfer.	0

16.4.2 Channel Interrupt Enable Register

Address: 0xF400_2C04

Bit	R/W	Description	Default value
31 : 2	R	Reserved	-
1 : 0	R/W	Disables/Enables interrupt 0 : Disable interrupt 1 : Enable interrupt	00

16.4.3 Channel Interrupt Status Register

Address: 0xF400_2C08

Bit	R/W	Description	Default value
31 : 2	R	Reserved	-
1:0	R/W	Status of the interrupt 0 : Not occurred 1 : Interrupt occurred	00

16.4.4 DMA Channel Interrupt Clear Register

Address: 0xF400_2C0C

Bit	R/W	Description	Default value
31 : 2	R	Reserved	-
1 : 0	R/W	Clear interrupt 0 : No Effect 1 : Interrupt Clear	00

16.4.5 Software Handshaking Register

Address: 0xF400_2C10

Bit	R/W	Description	Default value
31 : 8	R	Reserved	-
7 : 0	R/W	S/W DMA transfer Request. Automatically cleared by hardware at the completion of transfer.	00

16.4.6 Source Software Burst Transaction Request Register

Address: 0xF400_2C14

Bit	R/W	Description	Default value
31 : 8	R	Reserved	-
7 : 0	R/W	S/W Burst Transaction Request. Automatically cleared by hardware at the completion of transfer.	00

16.4.7 Destination Software Burst Transaction Request Register

Address: 0xF400_2C18

Bit	R/W	Description	Default value
31 : 8	R	Reserved	-
7 : 0	R/W	S/W Burst Transaction Request Automatically cleared by hardware at the completion of transfer.	00

16.4.8 Source Software Single Transaction Request Register

Address: 0xF400_2C1C

Bit	R/W	Description	Default value
31 : 8	R	Reserved	-
7 : 0	R/W	S/W Single Transaction Request. Automatically cleared by hardware at the completion of transfer.	00

16.4.9 Destination Software Single Transaction Request Register

Address: 0xF400_2C20

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7 : 0	R/W	S/W Single Transaction Request. Automatically cleared by hardware at the completion of transfer.	00

16.4.10 Source Software Last Transaction Request Register

Address: 0xF400_2C24

Bit	R/W	Description	Default value
31 : 8	R	Reserved	-
7 : 0	R/W	S/W Single Transaction Request. Automatically cleared by hardware at the completion of transfer.	00

16.4.11 Destination Software Last Transaction Request Register

Address: 0xF400_2C28

Bit	R/W	Description	Default value
31 : 8	R	Reserved	-
7 : 0	R/W	S/W Single Transaction Request. Automatically cleared by hardware at the completion of transfer.	00

16.4.12 Source Address Register

Address: 0xF400_2C80 / 0xF400_2CC0

Bit	R/W	Description	Default value
31 : 0	R/W	Source Address Register	0

16.4.13 Destination Address Register

Address: 0xF400_2C84/ 0xF400_2CC4

Bit	R/W	Description	Default value
31 : 0	R/W	Destination Address Raiser	0

16.4.14 Linked List Pointer Register

Address: 0xF400_2C88 / 0xF400_2CC8

Bit	R/W	Description	Default value
31 : 2	R/W	Linked list point register	0
1 : 0	R	Reserved	-

16.4.15 Channel Control 0 Register (ChnCntl)

Address: 0xF400_2C8C / 0xF400_2CCC

Bit	R/W	Description	Default value
31:20	R/W	Block Transfer Size(BLOCK_TS) The total number of single transactions to perform for every block transfer	0
19	R/W	DONE Software can poll this bit to see when a block transfer is complete	0
18	R/W	INT EN Channel interrupt enable	0
17		Source Gather enable (SRC_GATHER_EN)	0
16	R/W	Destination Scatter enable (DST_SCATTER_EN)	0
15:12	R/W	Source Burst Length(SRC_BLEN) Mapped to ARLEN or AWLEN. SRC_TR_WIDTH is the number of the transfer. 0011: this value should be available 000 : 1 100 : 5 001 : 2 101 : 6 010 : 3 110 : 7 011: 4 111 : 8	0

		1111:16	
11:10	R/W	Source Transfer Width, It is mapped to a single AXI AWSIZE, ARSIZE SRC_TR_WIDTH 00 : 8bits, 01 : 16bits, 10 : 32bits, 11 : 64bits	0
9:8	R	Source Increments(SINC) 00 : fixed 01 : Increment	0
7:4	R/W	Destination Burst Length(DST_BLEN) It is mapped to AXI ARLEN, AWLEN. The number of the transfer. 0011: this value is available. 000 : 1 100 : 5 001 : 2 101 : 6 010 : 3 110 : 7 011: 4 111 : 8 1111: 16	0
3:2	R/W	Destination Transfer Width -> Mapped to AWSIZE/ARSIZE of AXI Bus 00 : 8bits, 01 : 16bits, 10 : 32bits, 11 : 64bits	0
1:0	R/W	Destination Increments(DINC) 00 : fixed 01 : Increment	000

16.4.16 Channel Control 1 Register

Address: 0xF400_2C90 / 0xF400_2CD0

Bit	*R/W*	*Description*	*Default value*
31:27	R/W	Multi block count	0
26:24	R/W	Tr	000
23:20	R/W	MAX AXI Burst Length 0000 : 1 0001 : 2 … : … 1101 : 14 1110 : 15 1111 : 16	0
19	R/W	Linked-list enable(LL_EN) Both source and destination LL_EN bit must be enabled.	0
18	R/W	Multi block reload enable 1: Auto reload or contiguous	0
17	R/W	Multi block stall	0
16	R/W	Channel suspend(halt) bit	0
15	R/W	Reserved	-
14	R/W	SRC Channel Lock bit	0
13	R/W	SRC BUS Lock bit	0
12	R/W	Src contiguous + offset	0
11	R/W	Reserved	-
10:8	R/W	Reserved	-
7	R/W	Reserved	-
6	R/W	DST Channel Lock bit	0
5	R/W	DST BUS Lock bit	0
4	R/W	Dst contiguous + offset	0
3	R/W	Reserved	-
2:0	R/W	Reserved	-

16.4.17 Source Contiguous Offset Address Register

Address: 0xF400_2C94 / 0xF400_2CD4

Bit	*R/W*	*Description*	*Default value*
31 : 20	R	Reserved	-
19 : 0	R/W	Offset address for next block transfer	00

16.4.18 Destination Contiguous Offset Address Register

Address: 0xF400_2C98 / 0xF400_2CD8

Bit	R/W	Description	Default value
31 : 20	R	Reserved	-
19 : 0	R/W	Offset address for next block transfer	00

16.4.19 Status Register

Address: 0xF400_2C9C / 0xF400_2CDC

Bit	R/W	Description	Default value
31:8		Reserved.	-
7:0	R/W	Check the number of multi block transfer	0

16.4.20 Source Gather Register

Address: 0xF400_2CA0 / 0xF400_2CE0

Bit	R/W	Description	Default value
31 : 0	R/W	Reserved	-

16.4.21 Destination Scatter Register

Address: 0xF400_2CA4 / 0xF400_2CE4

Bit	R/W	Description	Default value
31 : 20	R/W	Reserved	-

17 Display Controller

17.1 Features

- Digital RGB[23:0] I/F
- Analog RGB I/F
- HDTV 720p I/F
- TV Encoder Interface
- BT656 Capture input interface
- 256x25bits palette for the overlay(win1)
- Supports Transparent Overlay(win1)
- Supports Color key function
- Window0
  - Support RGB(8:8:8) image data from frame buffer
  - Support RGB(5:6:5) image data from frame buffer
  - Support YcbCr(4:2:2) image data from frame buffer
- Window1(OSD)
  - Supports 4- or 8-BPP(bit per pixel) palletized color
  - Supports 16- or 24BPP non-palletized color
  - Supports 4- or 8-bit Alpha blending (Plane/Pixel)

17.2 Block Diagram

17.2.1 Display Controller

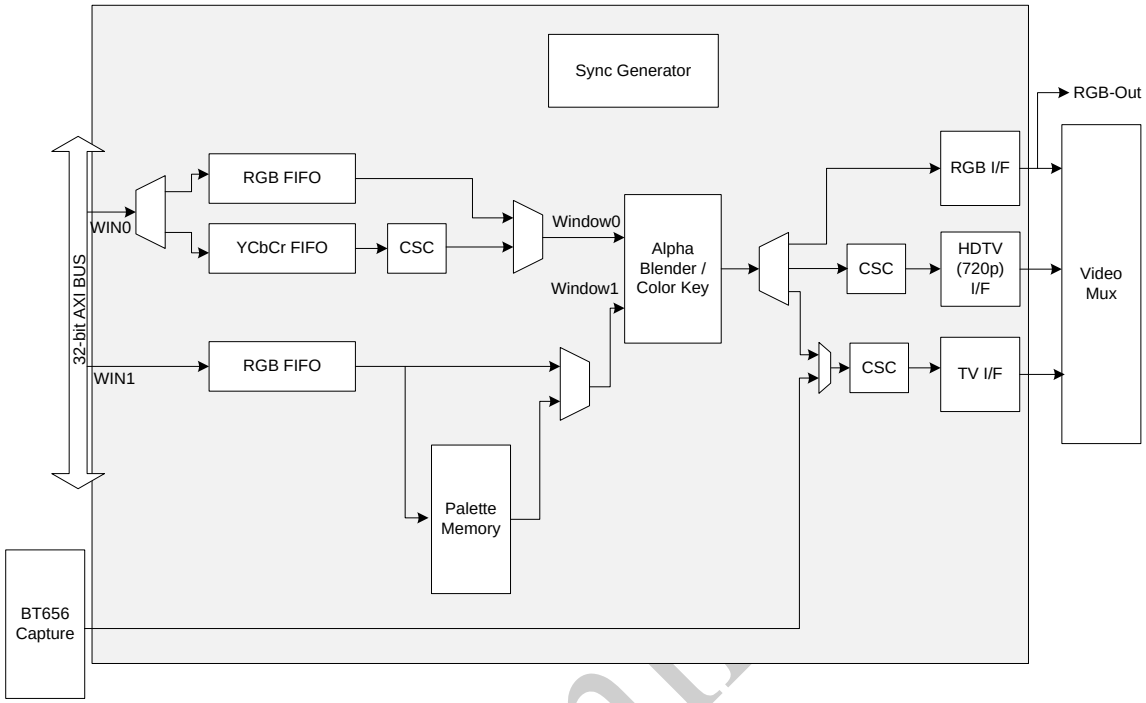


Figure 17-1 Display Controller Block Diagram

Figure 17-1 shows the block diagram of Display controller.

17.3 Output Data Flow

17.3.1 Display Controller interface to connection with external device

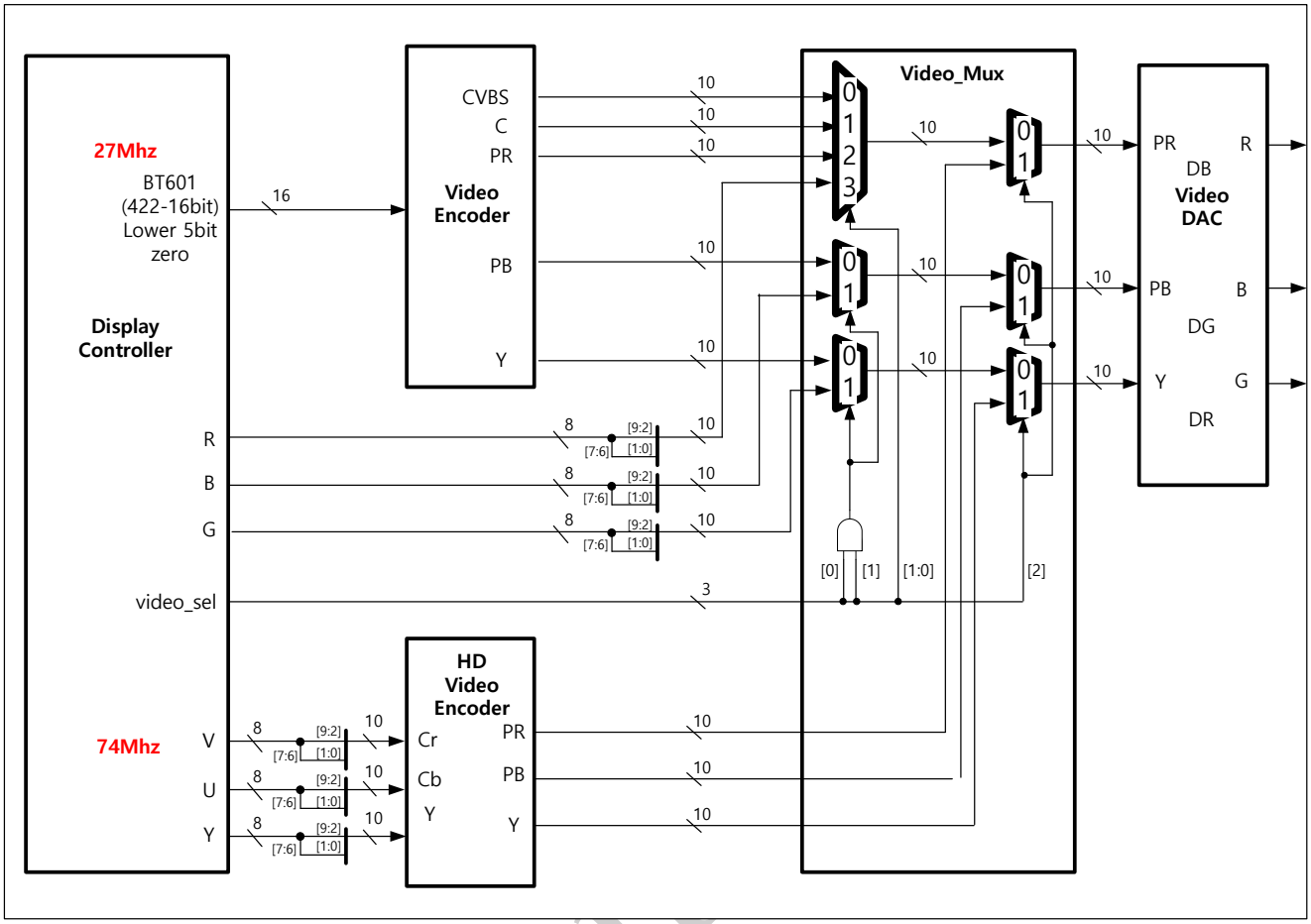


Figure 17-2 Block diagram of the Video Selector

Figure 17-2 shows that Display controller has connection with Video DAC, TV Encoder and HD TV encoder.

External connection is selected by the Window0 Control register' bit 29:27.

17.4 Window0 Layer

17.4.1 Window0 supported Color Format

The kind of input image is selected by Window0 Control register's bit 13:12.

Support format is following:

- YcbCr422 interlace
- RGB 16bit
- RGB 24bit
- YcbCr422 progressive

YcbCr422 interlace data should be loaded on the frame buffer like the below figure.

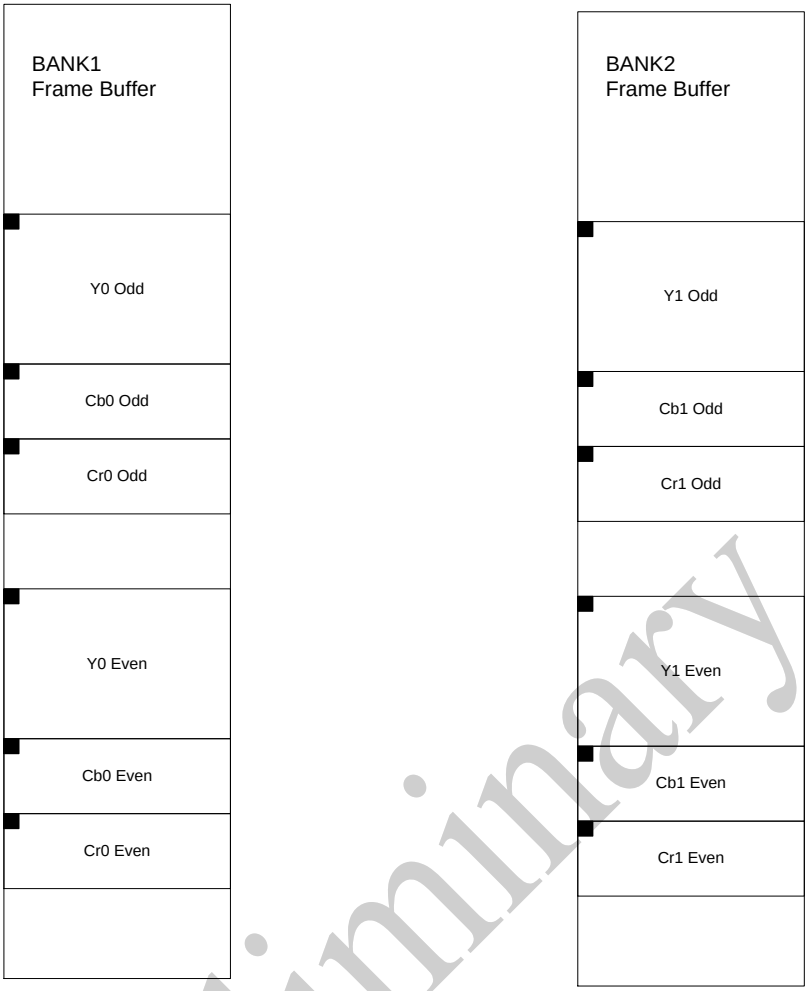
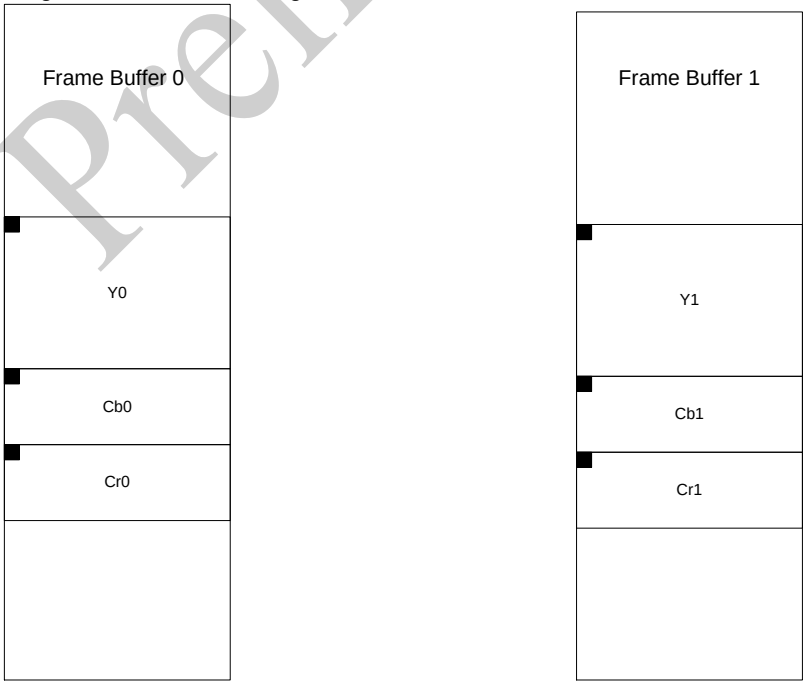


Figure 17-3 Block diagram of Ping-Pong architecture

The following diagram is YcbCr4:2:2 Progressive



RGB24bit format should include dummy 8bit.

	D[31:24]	D[23:0]
00H	Dummy	RGB Pixel1
04H	Dummy	RGB Pixel2
...	...	...

RGB16bit format

	D[31:16]	D[15:0]
00H	RGB Pixel2	RGB Pixel1
04H	RGB Pixel4	RGB Pixel3
...	...	...

17.5 Window1(OSD) Layer

17.5.1 Alpha layer

Pixel alpha enable bit	Alpha_value_sel bit	Comment
0 : Plane alpha (default mode)	0 : Alpha value0 register	
	1 : Alpha value1 register	
1 : Pixel alpha	0 : Image alpha enable, or alpha value	
	1 : Reserved	

17.5.2 Winodw1(OSD) Color format

17.5.2.1 32BPP display(A8+888)

Address	D[31:24]	D[23:0]
00H	Alpha value	Pixel1
04H	Alpha value	Pixel2
08H	Alpha value	Pixel3
…	…	…

Alpha value is four bits.
If pixel alpha is enabled, Alpha value[7:0] is used.

17.5.2.2 28BPP display(A4+888)

Address	D[31:28]	D[27:24]	D[23:0]
00H	Dummy bit	Alpha value1	Pixel1
04H	Dummy bit	Alpha value2	Pixel2
08H	Dummy bit	Alpha value3	Pixel3
…	…	…	…

Alpha value is four bits..
If pixel alpha is enabled, Alpha value[3:0]is used.

17.5.2.3 25BPP display(A+888)

Address	D[31:25]	D[24]	D[23:0]
00H	Dummy bit	AEN1	Pixel1
04H	Dummy bit	AEN2	Pixel2
08H	Dummy bit	AEN3	Pixel3
…	…	…	…

If pixel alpha is enabled, Alpha is :
AEN = 0, global alpha0 is used.
AEN =1, global alpha1 is used.

17.5.2.4 24BPP display(888)

Address	D[31:25]	D[23:0]
00H	Dummy bit	Pixel1
04H	Dummy bit	Pixel2
08H	Dummy bit	Pixel3
…	…	…

17.5.2.5 16BPP display(A555)

If pixel alpha is enabled, Alpha is :
AEN = 0, global alpha0 is used.
AEN =1, global alpha1 is used

Address	D[31]	D[30:16]	D[15]	D[14:0]
00H	AEN2	Pixel2	AEN1	Pixel1
04H	AEN4	Pixel4	AEN3	Pixel3
08H	AEN6	Pixel6	AEN5	Pixel5
…	…	…	…	…

17.5.2.6 16BPP display(565)

Address	D[31:16]	D[15:0]
00H	Pixel2	Pixel1
04H	Pixel4	Pixel3
08H	Pixel6	Pixel5
…	…	…

17.5.2.7 8BPP display(Palette)

Address	D[31:24]	D[23:16]	D[15:8]	D[7:0]
00H	Pixel4	Pixel3	Pixel2	Pixel1
04H	Pixel8	Pixel7	Pixel6	Pixel5
08H	Pixel12	Pixel11	Pixel10	Pixel9
…	…	…	…	…

17.5.2.8 4BPP display(Palette)

Address	D[31:28]	D[27:24]	D[23:20]	D[19:16]	D[15:12]	D[11:8]	D[7:4]	D[3:0]
00H	Pixel8	Pixel7	Pixel6	Pixel5	Pixel4	Pixel3	Pixel2	Pixel1
04H	Pixel16	Pixel15	Pixel14	Pixel13	Pixel12	Pixel11	Pixel10	Pixel9
08H	Pixel24	Pixel23	Pixel22	Pixel21	Pixel20	Pixel19	Pixel18	Pixel17
…	…	…	…	…	…	…	…	…

17.6 Palette Memory

17.6.1 Palette Memory Format

17.6.1.1 256 level, 16level

256 level is like the following:

Bit INDEX	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00H	AEN	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
01H	AEN	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
…	AEN	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
FFH	AEN	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0

If pixel alpha is enabled, Alpha is
AEN = 0, global alpha0 is used.
AEN =1, global alpha1 is used

In the 16level, lower 16 entry are available.

.

17.6.1.2 Access to Palette Memory

The address of pallet memory is automatically increasing every access.

17.7 Target Coordinate Configure

17.7.1 Target Coordinate configure

The ordering is as following:

Target Width,
Target Height,
Target Start X
Target Start Y (<- all register are properly set.)

17.7.2 OSD coordinate configure for TV-out

Target Y coordinate value must be odd, such as (0.0), (0.2)… (x, odd).

17.8 Resolution configuration

17.8.1 Bigger image output configure

To comply with Graphics engine, the resolution should be set such as 512x512, 1024x1024, 2048x2048 .

For 640x480 or 1024x1024, Pixel offset Register should be used.

The unit is pixel, The value is set by the difference image with and output width..

In the case 640 width, 1024 – 640 is set.

17.9 Register Description

17.9.1 DC TV Encoder Interface Register(DCTEI)

Address : 0xF400_1000h

Bit	R/W	Description	Default value
31 : 6	R	Reserved	-
5	R/W	TV Encoder S/W system reset_n 0 : reset 1 : normal state	0b
4	R/W	TV Encoder S/W register reset_n 0 : reset 1 : normal state	0b
3 : 2	R	Reserved	-
1	R/W	CB CR order selection	0b
0	R/W	0 : Field_DVALID port is Data Valid signal(HAV & VAV/Active High) 1 : Field_DVALID port is Field Information	0b

17.9.2 DC Horizontal Total Register (DCHT)

Address : 0xF400_1004h

Bit	R/W	Description	Default value
31 : 11	R	Reserved	-
10 : 0	R/W	Horizontal Total The value loaded into this filed is the total pixel counts per line.	000h

* Horizontal Total scan value include Horizontal Active and Blank

17.9.3 DC Horizontal Sync. Start / End Register(DCHS)

Address : 0xF400_1008h

Bit	R/W	Description	Default value
31 : 27	R	Reserved	-
26 : 16	R/W	Horizontal Sync Start The value loaded into this field is the value of horizontal sync period start by the horizontal counter	000h
15 : 11	R	Reserved	-
10 : 0	R/W	Horizontal Sync End The value loaded into this filed is the value of horizontal sync period start by the horizontal counter	000h

* Start(End) value during Horizontal Sync

17.9.4 DC Horizontal Active Start / End Register(DCHA)

Address : 0xF400_100Ch

Bit	R/W	Description	Default value
31 : 27	R	Reserved	-
26 : 16	R/W	Horizontal Active Start The value loaded into this field is the value of horizontal active period start by the horizontal counter	000h
15 : 11	R	Reserved	-
10 : 0	R/W	Horizontal Active End The value loaded into this filed is the value of horizontal active period start by the horizontal counter	000h

* Start(End) value during Horizontal Active

17.9.5 DC Vertical Total Register(DCVT)

Address : 0xF400_1010h

Bit	R/W	Description	Default value
31 : 11	R	Reserved	-
10 : 0	R/W	Vertical Total The value loaded into this field is the value of the total vertical lien counts	000h

* Vertical Total scan value includes Vertical Active and Blank

17.9.6 DC Vertical Sync. Start / End Register(DCVS)

Address : 0xF400_1014h

Bit	R/W	Description	Default value
31 : 27	R	Reserved	-
26 : 16	R/W	Vertical Sync Start The value loaded into this field is the value of vertical sync period start by the	000h

		horizontal counter	
15 : 11	R	Reserved	-
10 : 0	R/W	Vertical Sync End The value loaded into this filed is the value of vertical sync period start by the horizontal counter	000h

* Start(End) value during Vertical Sync

17.9.7 DC Vertical Active Start / End Register(DCVA)

Address : 0xF400_1018h

Bit	*R/W*	*Description*	*Default value*
31 : 27	R	Reserved	-
26 : 16	R/W	Vertical Active Start The value loaded into this field is the value of vertical active period start by the horizontal counter	000h
15 : 11	R	Reserved	-
10 : 0	R/W	Vertical Active End The value loaded into this filed is the value of vertical active period start by the horizontal counter	000h

* Start(End) value during Vertical Active

17.9.8 DC Display Current X / Y Position Register(DCXY)

Address : 0xF400_101Ch

Bit	*R/W*	*Description*	*Default value*
31 : 27	R	Reserved	-
26 : 16	R	The value loaded into this field is the value of the vertical counter.	000h
15 : 11	R	Reserved	-
10 : 0	R	The value loaded into this field is the value of the horizontal counter.	000h

17.9.9 DC Status Register(DCSTAT)

Address : 0xF400_1020h

Bit	*R/W*	*Description*	*Default value*
31 : 16	R	Reserved	-
15 : 8	R	Check Palette memory address, when read access to this register palette memory address is cleared.	0h
7 : 6	R	Reserved	-
5	R	Current Base Address	0b
4	R	Reserved	-
3	R	Vertical Active (active high)	0b
2	R	Vertical Sync	1b
1	R	Horizontal Active (active high)	0b
0	R	Horizontal Sync	1b

17.9.10 DC Window0 Control Register(DCW0C)

Address : 0xF400_1024h

Bit	*R/W*	*Description*	*Default value*
31 : 30	R	Reserved	-
29 : 27	R/W	Video Output Selection 000 : CVBS (TV out) 001 : Reserved 010 : SD YpbPr (TV out) 011 : Analog RGB (Display Control Out) 100 : HD YpbPr (HDTV out)	000b
26 : 25	R	Reserved	00b
24	R/W	Window0 Enable 0 : Disable 1 : Enable	0b
23 : 22	R	Reserved	-
21	R/W	HSYNC. Output Polarity 0 : LOW ACTIVE 1 : HIGH ACTIVE	0b
20	R/W	VSYCNC. Output Polarity 0 : LOW ACTIVE 1 : HIGH ACTIVE	0b
19 : 14	R	Reserved	0b
13 : 12	R/W	Input Source Format 00 : YCbCr422 Interlace	00b

		01 : RGB 16bit 10 : RGB 32 bit 11 : YcbCr422 Progressive	
11 : 10	R	Reserved	-
9	R/W	Capture Direct connect mode 1 : directly connected capture	0b
8	R	Reserved	-
7	R/W	TV-Out 0 : RGB-Out/HDTV-Out 1 : TV Out	0b
5	R/W	Apply vertical real cout value for vertical sync generation for HD TV out	0b
4 : 2	R	Reserved	0b
1 : 0	R/W	Screen Display Mode Control. 00 : Normal Operation 01 : Regular Pattern Generation 1x : Screen off	00b

* Display Control register is used to control the operation of DC. function

17.9.11 DC VESA Power Management(DCPM)

Address : 0xF400_102Ch

Bit	R/W	Description	Default value
31 : 2	R	Reserved	-
1 : 0	R/W	VESA Power Management Control	00b

1 0	Stage	Vsync	Hsync
0 0	On	On	On
0 1	Stand-by	On	Off
1 0	Suspend	Off	On
1 1	Off	Off	Off

17.9.12 DC Frame Number Register(DCFNR)

Address : 0xF400_1038h

Bit	R/W	Description	Default value
31 : 0	R/W	Frame Number	000h

17.9.13 DC Y0 Start Address Register (DCY0S)

Address : 0xF400_1040h

Bit	R/W	Description	Default value
31 : 0	R/W	Y0 Start Address or Y0 Odd start address	00h

17.9.14 DC Y0 Even Start Address Register (DCY0ES)

Address : 0xF400_1044h

Bit	R/W	Description	Default value
31 : 0	R/W	Y0 Even Start Address	00h

17.9.15 DC CB0 Start Address (DCCB0S)

Address : 0xF400_1048h

Bit	R/W	Description	Default value
31 : 0	R/W	Cb0 Start Address or Cb0 Odd start address	00h

17.9.16 DC CB0 Even Start Address (DCCB0ES)

Address : 0xF400_104Ch

Bit	R/W	Description	Default value
31 : 0	R/W	Cb0 Even Start Address	00h

17.9.17 DC CR0 Start Address Register (DCCR0S)

Address : 0xF400_1050h

Bit	R/W	Description	Default value
31 : 0	R/W	Cr0 start address or Cr0 Odd start address	00h

17.9.18 DC CR0 Even Start Address Register (DCCR0ES)

Address : 0xF400_1054h

Bit	R/W	Description	Default value
31 : 0	R/W	Cr0 Even start address	00h

17.9.19 DC Y1 Start Address Register (DCY1S)

Address : 0xF400_1058h

Bit	R/W	Description	Default value
31 : 0	R/W	Y1 Start Address or Y1 Odd start address	00h

17.9.20 DC Y1 Even Start Address Register (DCY1ES)

Address : 0xF400_105Ch

Bit	R/W	Description	Default value
31 : 0	R/W	Y1 Even Start Address	00h

17.9.21 DC CB1 Start Address Register (DCCB1S)

Address : 0xF400_1060h

Bit	R/W	Description	Default value
31 : 0	R/W	Cb1 Start Address or Cb1 Odd start address	00h

17.9.22 DC CB1 Even Start Address Register (DCCB1ES)

Address : 0xF400_1064h

Bit	R/W	Description	Default value
31 : 0	R/W	Cb1 Even Start Address	00h

17.9.23 DC CR1 Start Address Register (DCCR1S)

Address : 0xF400_1068h

Bit	R/W	Description	Default value
31 : 0	R/W	Cr1 start address or Cr1 Odd start address	00h

17.9.24 DC CR1 Even Start Address Register (DCCR1ES)

Address : 0xF400_106Ch

Bit	R/W	Description	Default value
31 : 0	R/W	Cr1 Even start address	00h

17.9.25 DC Window1 Base 0 Address Register(DCW1BA0)

Address : 0xF400_1070h

Bit	R/W	Description	Default value
31 : 0	R/W	base address 0	00h

17.9.26 DC Window1 Base 1 Address Register(DCW1BA1)

Address : 0xF400_1074h

Bit	R/W	Description	Default value
31 : 0	R/W	base address 1	00h

17.9.27 DC Window1 Image width Register(DCW1IW)

Address : 0xF400_1078h

Bit	R/W	Description	Default value
31 : 0	R/W	Image Width	00h

17.9.28 DC Window1 Image Height Register(DCW1IH)

Address : 0xF400_107Ch

Bit	R/W	Description	Default value
31 : 0	R/W	Image Height	00h

17.9.29 DC Window1 Target Start X Register(DCW1X)

Address : 0xF400_1080h

Bit	R/W	Description	Default value
31 : 0	R/W	Target Start X	00h

17.9.30 DC Window1 Target Start Y Register(DCW1Y)

Address : 0xF400_1084h

Bit	R/W	Description	Default value
31 : 0	R/W	Target Start Y	00h

17.9.31 DC Window1 Palette Memory Register(DCW1PM)

Address : 0xF400_1088h

Bit	R/W	Description	Default value
31 : 0	R/W	If 8BPP, write 256 times. If 4BPP, read 16 times. Cleared by the read access to status register. When checking, If 8BPP, read 256 times. If 4BPP, read 16 times.	00h

17.9.32 DC Window1 Control Register(DCW1CNTL)

Address : 0xF400_108Ch

Bit	R/W	Description	Default value
31 : 25	R	Reserved	-
24	R/W	0: window1 disable, 1 : window1 enable	0b
23 : 16	R	Reserved	-
15:12	R/W	Image format selection. 1111: A8+888 1110 : A4+888 1101 : A888 1100 : 888 1011 : A555 1010 : 565 1001 : 8BPP(Bits Per Pixel) , Palette, Alpha 1000 : 8BPP, Palette 0111 : 4BPP, Palette, Alpha 0110 : 4BPP, Palette	-
11 : 10		Reserved	-
9		Colorkey enable 0: disable 1: enable	0
8 : 5	R	Reserved	-
4	R/W	DC Frame width selection 1 : Configurable with CRT Horizontal width register(Any Size) 0 : Fixed with 1024 pixels	0b
3	R/W	Alpha value sel 0: alpha value reg0 1: alpha value reg1 When pixel alpha is enabled, this value is not meaning. 0:AEN or alpha is used 1: Reserved	0b
2	R/W	Reserved	0b
1	R/W	Pixel alpha enable 0 : plane (default) 1 : pixel	0b
0	R/W	Reserved	0b

17.9.33 DC Window1 Global Alpha Value0 Register(DCW1GA0)

Address : 0xF400_1090h

Bit	R/W	Description	Default value
31 : 8	R/W	Reserved	-
7 : 0	R/W	Alpha value0	0

17.9.34 CRT Window1 Color Key Value Register (DCW1CK)

Address : 0xF400_1094h

Bit	R/W	Description	Default value
31 : 24	R/W	Reserved	-
23 : 0	R/W	Color Key (RGB)	0

17.9.35 DC Window1 Target Width Register (DCW1TW)

Address : 0xF400_10A0h

Bit	R/W	Description	Default value
31 : 2	R/W	Target width	00h

17.9.36 DC Window1 Target Height Register(DCW1TH)

Address : 0xF400_10A4h

Bit	R/W	Description	Default value
31 : 2	R/W	Target Height	00h

17.9.37 DC Window0 BANK 0 Address Register (DCBA0)

Address : 0xF400_10A8h

Bit	R/W	Description	Default value
31 : 2	R/W	Bank0 address	00h

17.9.38 DC Window0 BANK 1 Address Register(DCBA1)

Address : 0xF400_10ACh

Bit	R/W	Description	Default value
31 : 2	R/W	Bank1 address	00h

17.9.39 DC Window0 BANK 2 Address Register(DCBA2)

Address : 0xF400_10B0h

Bit	R/W	Description	Default value
31 : 2	R/W	Bank2 address	00h

17.9.40 DC Window0 BANK 3 Address Register (DCBA3)

Address : 0xF400_10B4h

Bit	R/W	Description	Default value
31 : 2	R/W	Bank3 address	00h

17.9.41 DC Window 0 Flip Enable / Status Register (DCW0FS)

Address : 0xF400_10B8h

Bit	R/W	Description	Default value
31 : 5	R/W	Reserved	-
9:8	R	Frame num[1:0] 00 : BANK0 : ycbcr bank0 01 : BANK1 : ycbcr bank1 10 : BANK2 : ycbcr bank0 11 : BANK3 : ycbcr bank1	00
7:5	R	Reserved	
4	R/W	Window 0 Flip Enable	0
3	R	Reserved	-
2	R/W	Window 0 Flip Enable S/W	0
1	R/W	Window 0 Flip Enable Graphics	0
0	R	Capture Flip Enable. (Ycbcr(i), RGB)	0

17.9.42 DC Window 0 Flip Control Register(DCW0FC)

Address : 0xF400_10BCh

Bit	R/W	Description	Default value
31 : 1	R/W	Reserved	-
0	R/W	Software flip request It is automatically clear at the end of the operation.	0

17.9.43 DC Version Register (DCV)

Address : 0xF400_10C0h

Bit	R/W	Description	Default value
31 : 8	R/W	Reserved	-
7 : 0	R/W	1.3 // Ver 1.3	0

17.9.44 DC Window1 Global Alpha Value1 (DCW1GA1)

Address : 0xF400_10C4h

Bit	R/W	Description	Default value
31 : 8	R/W	Reserved	-
7 : 0	R/W	Alpha value1	0

17.9.45 DC Window1 Flip Enable and Status Register (DCW1FS)

Address : 0xF400_10C8h

Bit	R/W	Description	Default value
31 : 10	R/W	Reserved	-
9:8	R	Frame Number, Bit9 is not used 00 : bank0 01 : bank1 10 : bank0 11 : baink1	0
4	R/W	Flip Enable	0
3	R	Reserved	-
2	R/W	S/W enable	0
1:0	R	Reserved	-

17.9.46 DC Window1 Flip Control Register (DCW1FC)

Address : 0xF400_10CCh

Bit	R/W	Description	Default value
31 : 1	R/W	Reserved	-
0-	R/W	S/W Flip request Only write possible	0

17.9.47 DC Window0 Pixel Offset Register (DCW0OFF)

Address : 0xF400_10D0h

Bit	R/W	Description	Default value
31 : 12	R/W	Reserved	-
11 : 2	R/W	When image size larger than resolution, used	0
1 : 0	R/W	Reserved	-

17.9.48 DC Window1 Pixel Offset Register (DCW1OFF)

Address : 0xF400_10D4h

Bit	R/W	Description	Default value
31 : 12	R/W	Reserved	-
11 : 2	R/W	When image size larger than resolution, used	00h
1 : 0	R/W	Reserved	-

18 SD Video Encoder

- Composite
- S-Video
- Component: RGB, YpbPr
- NTSC/PAL: 480/576 Interlaced

18.1 Features

- NTSC and PAL formats
- 16bit ITU-R BT.656/601 YCbCr(4:2:2) input format
- Composite(CVBS),S-Video(YC),Component(YPbPr) outputs
- APB Bus Interface

18.2 Block Description

18.2.1 top block

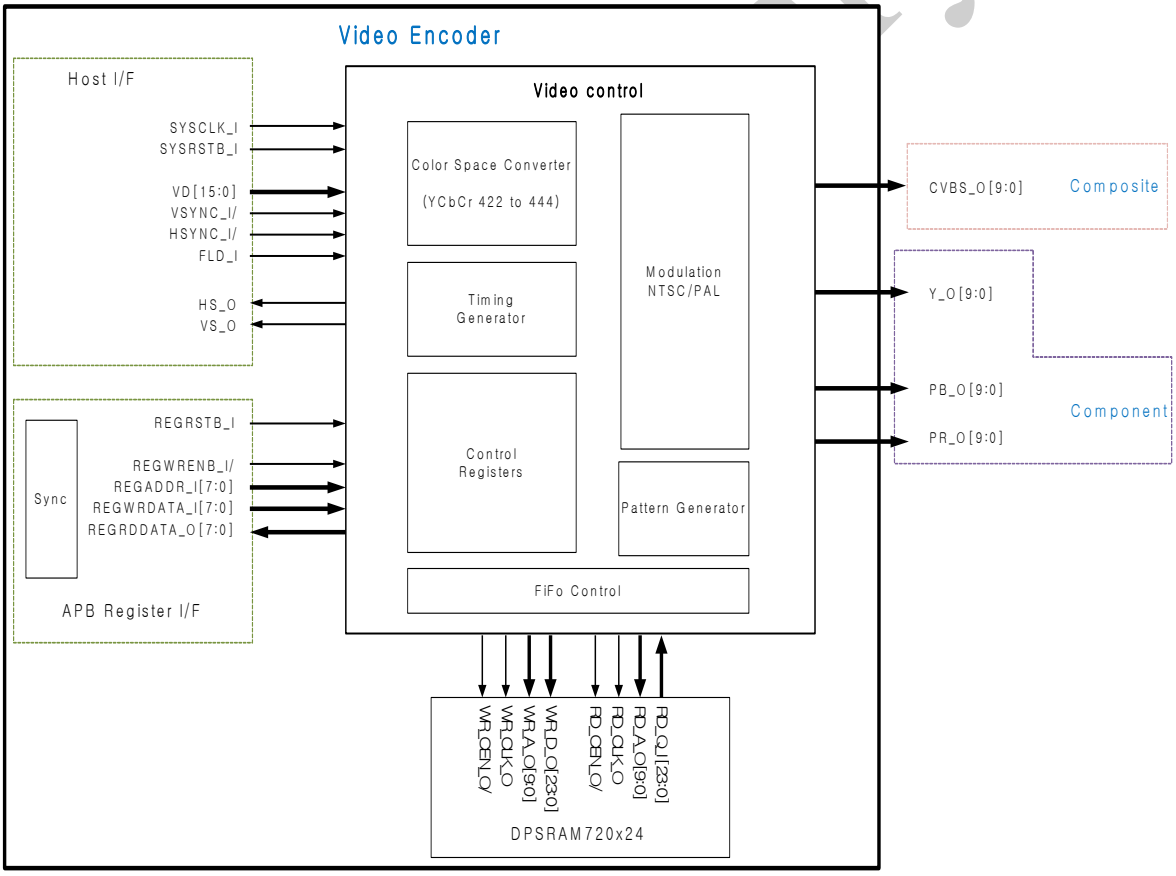


Figure 18-1 Video Encoder Block Diagram

18.2.2 apb to register sync interface

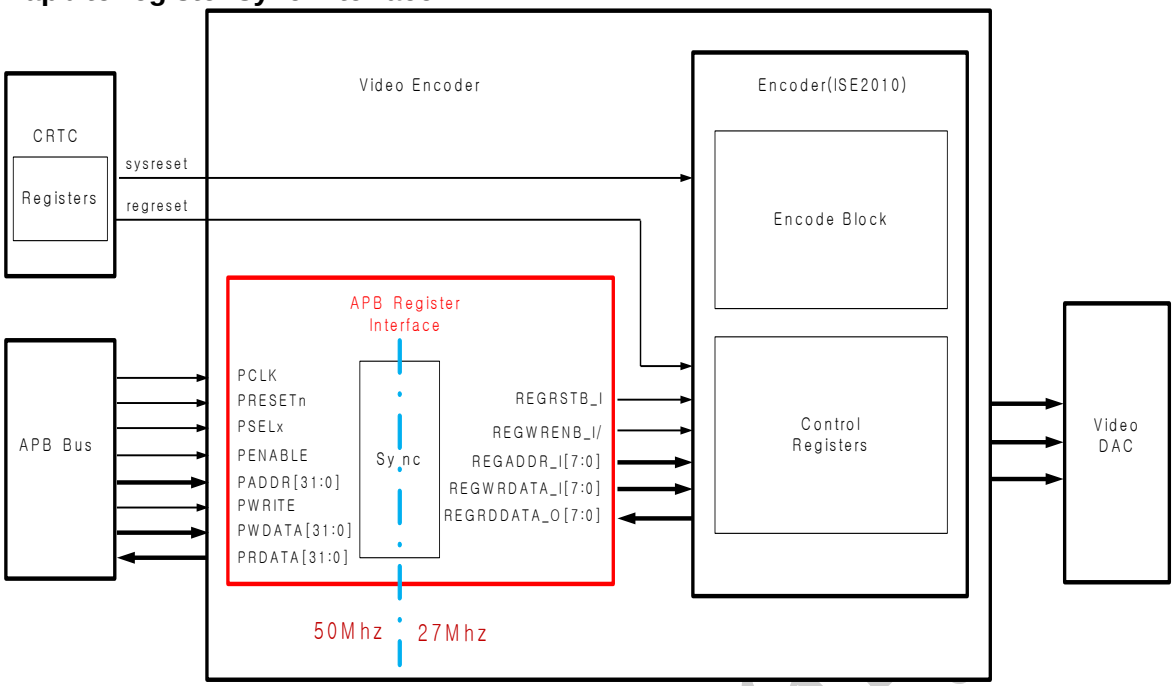


Figure 18-2 APB to Register I/F Sync

18.3 Function Description

18.3.1 Video Encoder clock

A 27Mhz is clocked from the PLL or external Video clock and BT656 ICE clock.

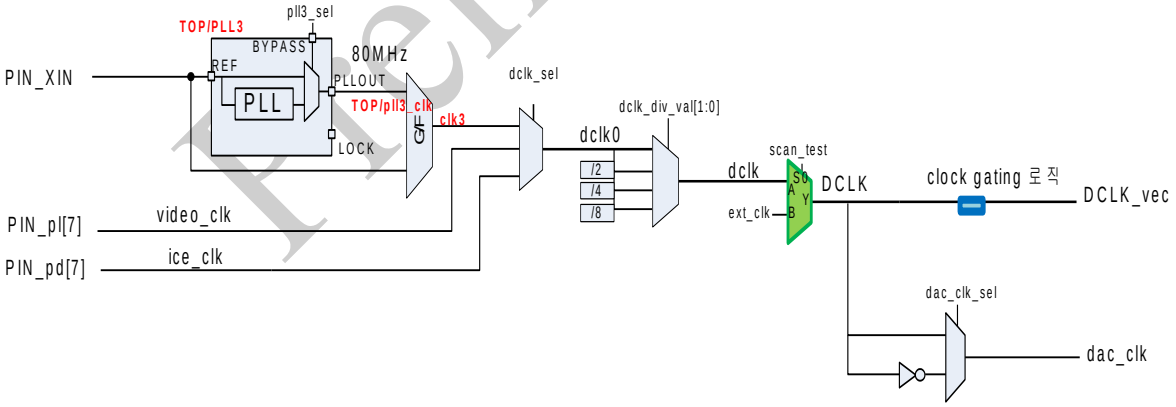


Figure 18-3 Video Encoder Clock

18.3.2 Video Encoder Reset

Video Encoder is avaliable when System reset_n and Register reset_n of System reset_n are released.

CRTC Address : xx00h

Bit	*R/W*	*Description*	*Default Value*
5	R/W	System reset_n 0 : reset 1 : normal state	0h
4	R/W	Register reset_n 0 : reset 1: normal state	0h

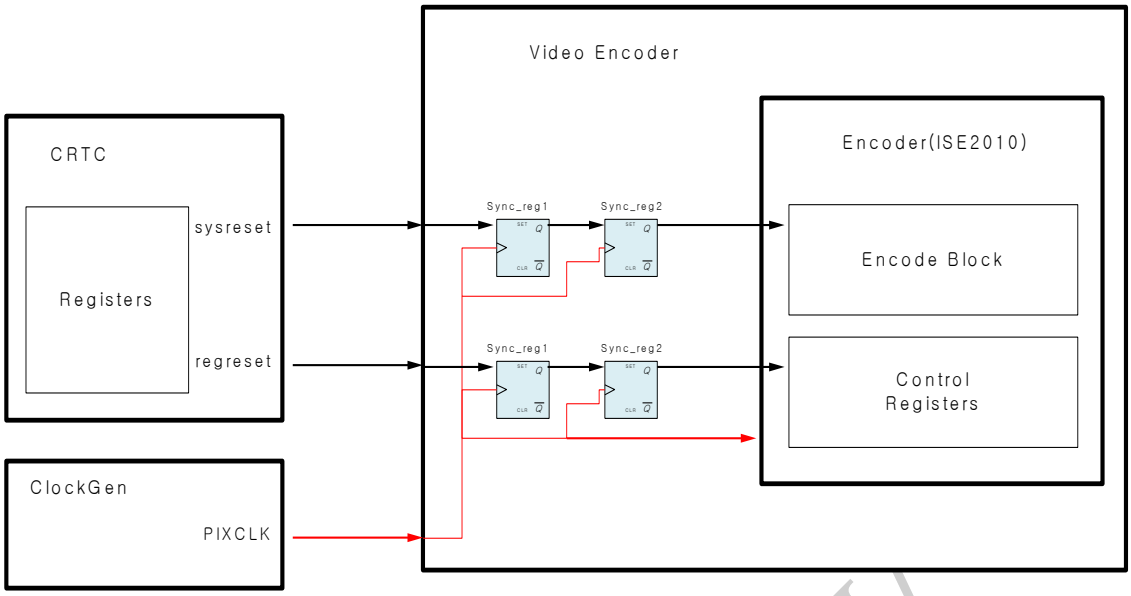


Figure 18-3 Video Encoder Reset

18.3.3 Setting Example

* CRTC (Rset) -> SDTV(Reset)
  *((volatile unsigned int *)0xf4001000) = 0x30; // Video Encoder Reset

* BT656 -> CRTC (Direct) -> SDTV (NTSC)
  *((volatile unsigned int *)0xf4002440) = 0x82; // 656,60Hz,DataValid
  *((volatile unsigned int *)0xf4002444) = 0x02; // Extracted by input EAV & SAV
  *((volatile unsigned int *)0xf400246C) = 0x03; // Input Signal Polarity Field inv

* BT601 -> CRTC -> SDTV (NTSC)
  *((volatile unsigned int *)0xf4002440) = 0x93; // 601,60Hz,FID
  *((volatile unsigned int *)0xf4002448) = 0x07; // gen hav_on,vav_on,fd_on BT601

* SDTV Color Bar (NTSC)
  *((volatile unsigned int *)0xf4002440) = 0x93; // 601,60Hz,FID
  *((volatile unsigned int *)0xf4002448) = 0x07; // gen hav_on,vav_on,fd_on BT601
  *((volatile unsigned int *)0xf4002480) = 0x01; // Pattern Gen On

* Offset Address 0x3FC is APB BUS' Status Register

19 HD Video Encoder

19.1 Features

- Input : SMPTE-296M compatible Y/Cb/Cr, 4:4:4 format (10bit)
- Input Sync : H/V SYNC signal (CEA-861-B, optional DV)
- Output : HDY/HDPB/HDPR (Progressive Mode Sync EIA-770.3-C, 1280x720p)
- Clock : 74.25Mhz
- Internal Color –bar Generator
- Adjustable Y/Pb/Pr Delay Function

19.2 Block Diagram

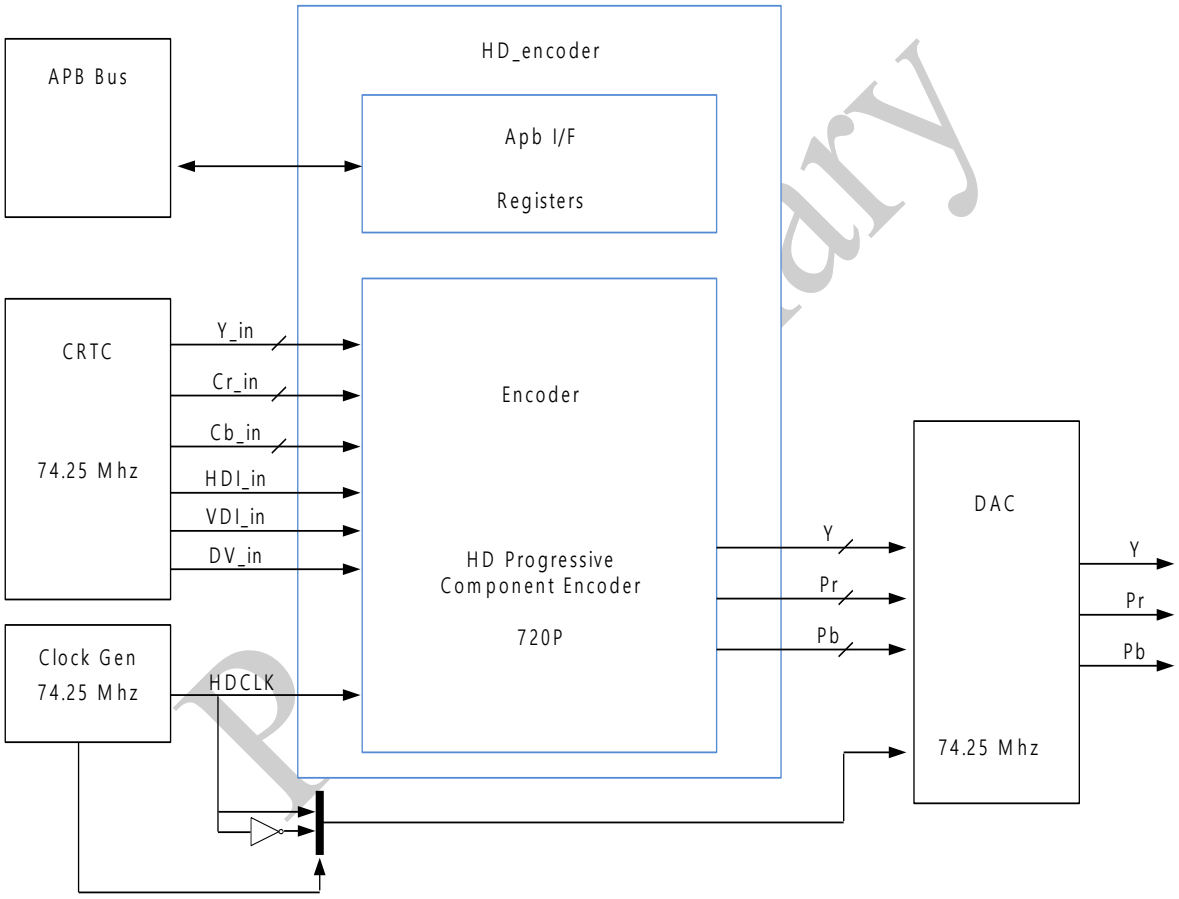


Figure 19-1 HD Video Encoder Block Diagram

19.3 Function Description

19.3.1 YCbCr 30bit Data Input Format

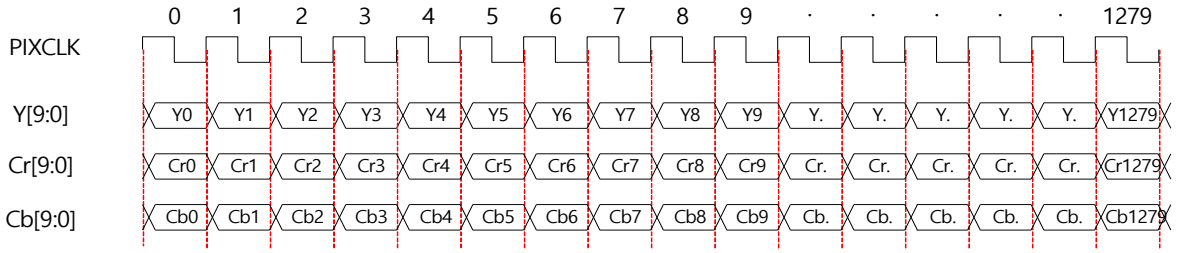


Figure 19-2 YCbCr 444 Input Data Format

19.3.2 Video Interface Timing

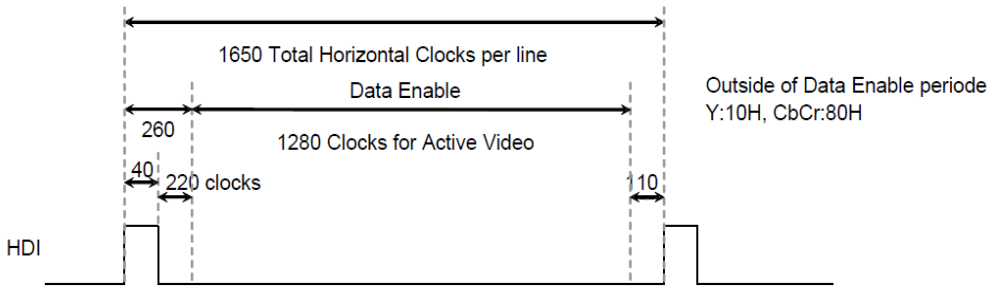


Figure 19-3 Input Video Data Hsync Timing

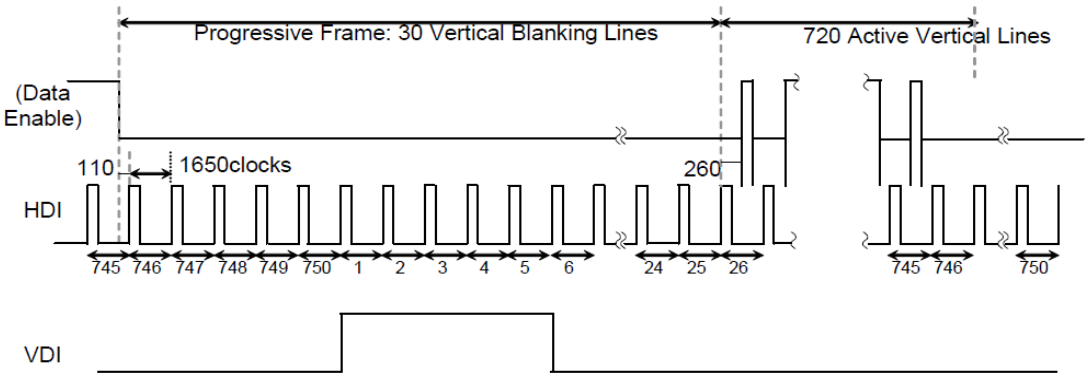
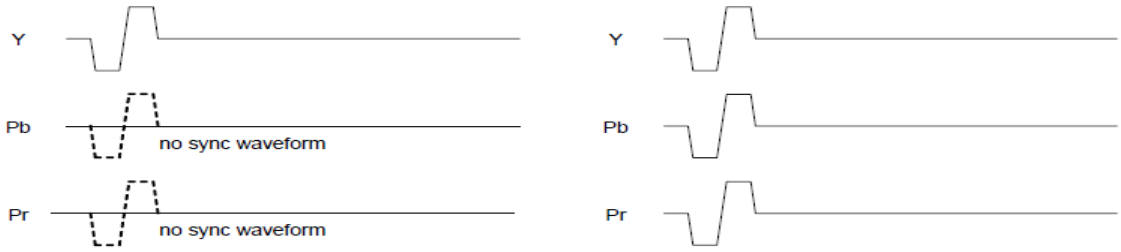


Figure 19-4 Input Video data Vsync Timing



syn_color = 1 **syn_color = 0**

Figure 19-5 Output Video Data Synchronization Pb/Pr Option Enable

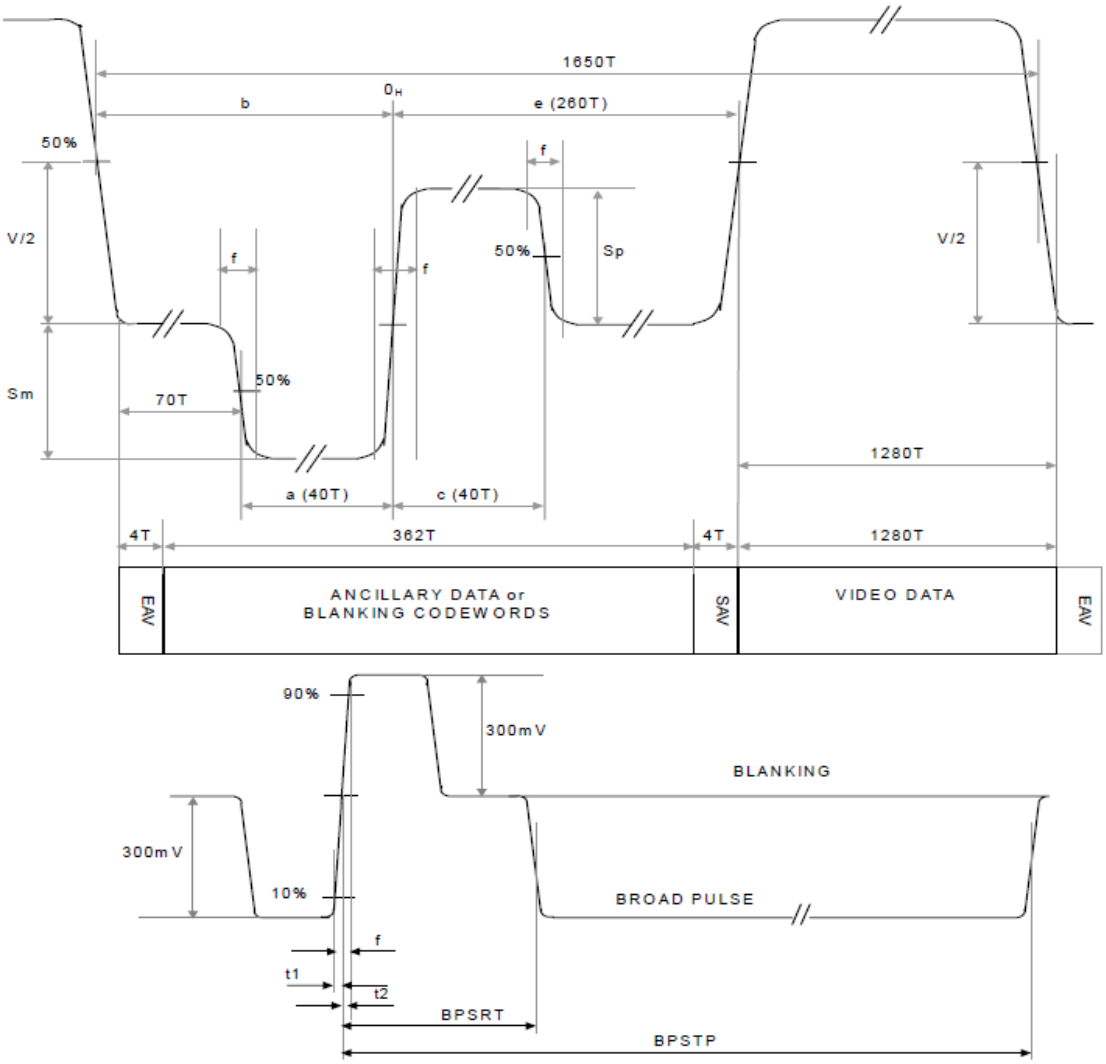


Figure 19-6 Output Video Data HSync Timing (60Mhz)

Symbol	parameter	Nominal value	Reference clock Interval	Tolerance CLK	Tolerance
a	Negative line sync width	0.539 [usec]	40	+/- 3	+/- 0.040 [usec]
b	End of active video	*1.495* [usec]	*111*		+0.080 [usec]
c	positive line sync width	0.539 [usec]	40	+/- 3	+/- 0.040 [usec]
e	Start of active video	3.502 [usec]	260	-0 / + 6	+0.080 [usec]
f	Rise/fall time	0.054 [usec]	4	+/- 1.5	+/- 0.020 [usec]
t2 – t1	Symmetry of rising edge	-	-		+/- 0.002 [usec]
Sm	Amplitude of negative pulse	300 [mV]	-		+/- 6mV
Sp	Amplitude of positive pulse	300 [mV]	-		+/- 6mV
V	Amplitude of video signal	700 [mV]	-		
	Total Lines		1650		
	Active Lines		1280	-12, +0	
BPSRT	Broad Pulse Start pos		260	0 ~ +6	+0.080 [usec]
BPSTP	Broad Pulse stop pos		1540	-6 ~ 0	- 0.080 [usec]

Figure 19-7 Output Video Data HSync table (60Mhz)

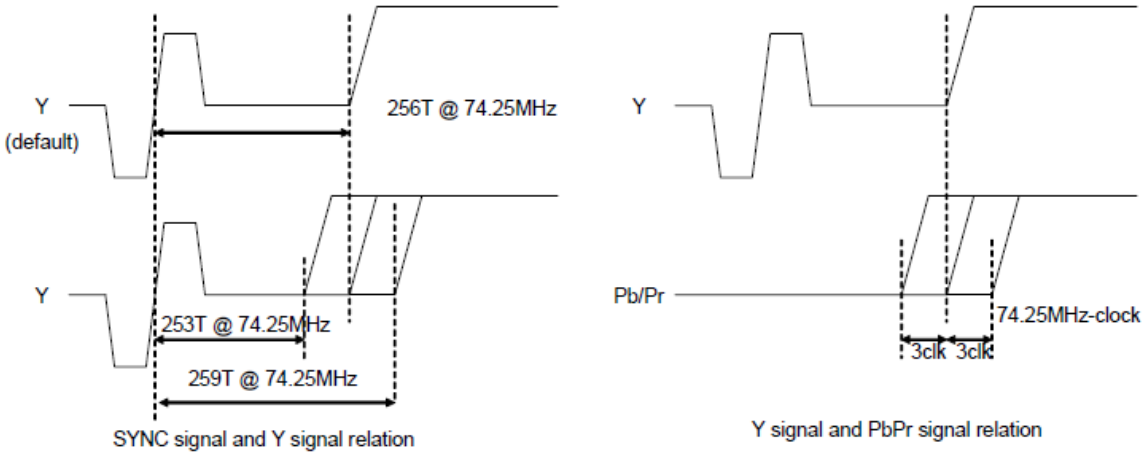


Figure 19-8 Output Video Data HSync table (60Mhz)

19.3.3 Video Data Output Level

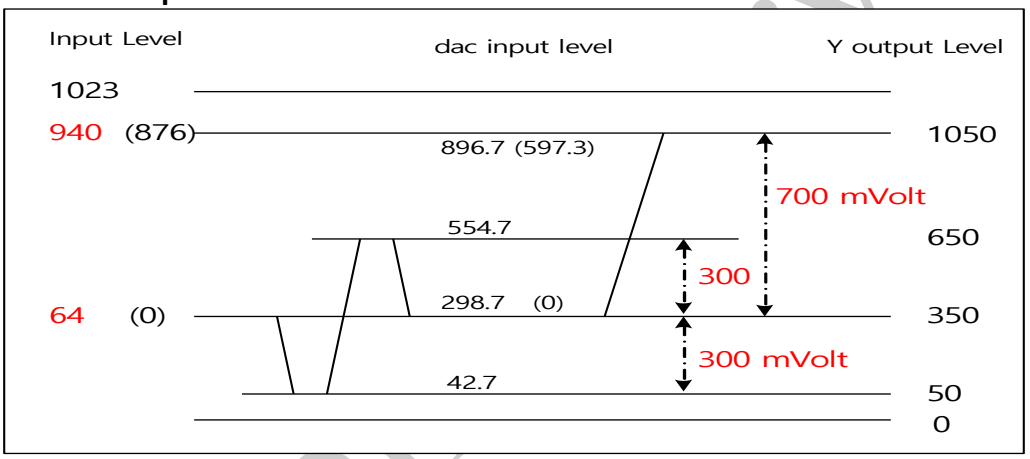


Figure 19-9 Output Y Level

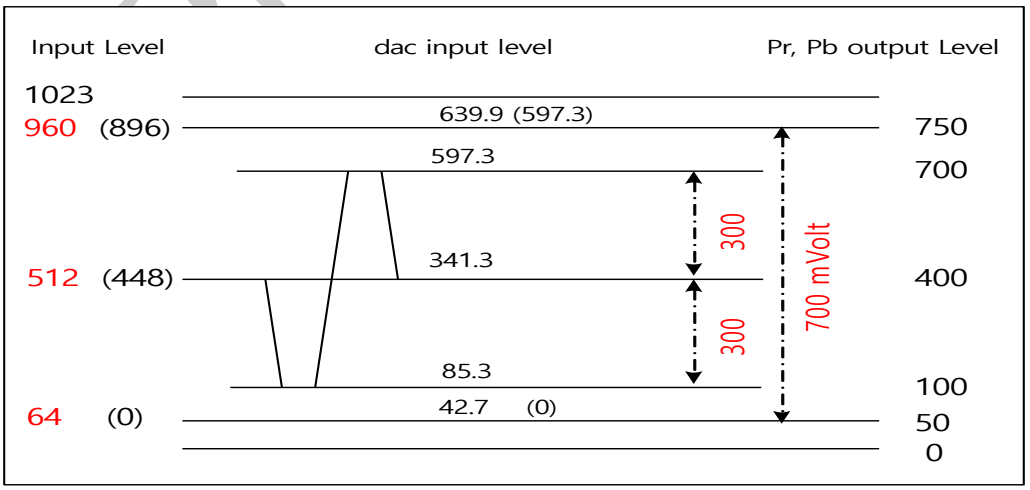


Figure 19-10 Output Pb/Pr Level

19.3.4 HD Video Setting Reference

When 10 Bit DAC ' s Ref Voltage is 1.2Volt : 1200 / 1024 = 1.171875 Step (Blue font : HD Encoder Reset Value)

Output 1050 / 1.171875 = 896 Level
Output 700 / 1.171875 = 597.33333333 Level
Output 300 / 1.171875 = 256 Level
Output 50 / 1.171875 = 42.66666666 Level

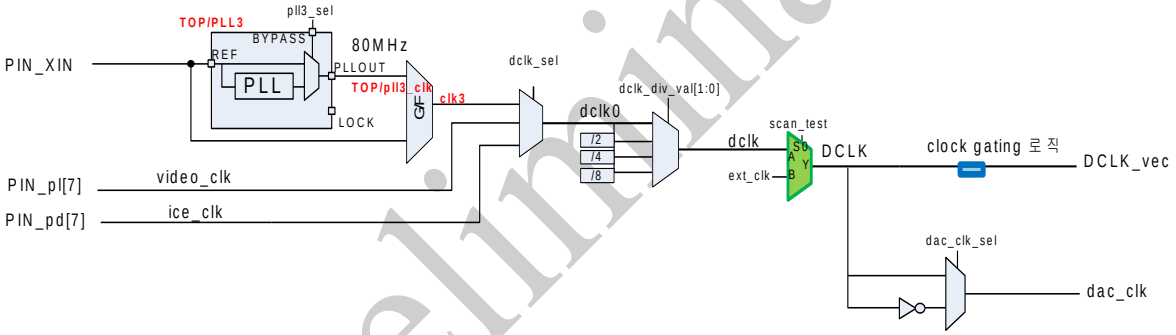
Y Input to DAC input Ratio
597.3 / 876 = 0.681849315
16bit Hex(4bit int, 12bit fraction) = 0x0ae9
Sync High Level : 555
Sync Level : 299
Sync Low Level : 43
Y Data DAC Offset Val
298.7 / 0.0681849315 = 438.073330029
= 438

Output 750 / 1.171875 = 640 Level
Output 700 / 1.171875 = 597.33333333 Level
Output 300 / 1.171875 = 256 Level
Output 50 / 1.171875 = 42.66666666 Level

Pr, Pb Input to DAC input Ratio
597.3 / 896 = 0.666666667
16bit Hex(4bit int, 12bit fraction) = 0x0aab
Sync High Level : 597
Sync Level : 341
Sync Low Level : 85
Pr, Pb Data DAC Offset Val
42.7 / 0.666666667 = 63.999999958
= 64

19.3.5 HD Video Encoder Clock

A 74.25Mhz is HD clocked from the PLL or external Video clock.



19.3.6 HD Video Setting Example

* CRTC -> HDTV (YPbPr)
  *((volatile unsigned int *)0xf4002800) = 0x00000001; // HD Enable

* HDTV Color Bar (YPbPr)
  *((volatile unsigned int *)0xf4002800) = 0x00010001; // HD Enable, Color Bar

19.4 Register Description

Address : 0xF400_2800

Bit	R/W	Description	Default value
31:25	R	Reserved	-
24	R/W	Pb, Pr sync enable 1 : enable 0 : disable	0
23:21	R	Reserved	-
20	R/W	VBI Data Insertion Enable (6~25Line) 1 : enable 0 : disable	0
19:17	R	Reserved	-
16	R/W	Test Color Bar Pattern Generator 1 : enable 0 : disable	0
15:13	R	Reserved	-
12	R/W	HD Data Valid Polarity 1 : low active 0 : high active	0
9:11	R	Reserved	-
8	R/W	Vertical Polarity 1 : low active 0 : high active	0
7:5	R	Reserved	-
4	R/W	Horizontal Polarity 1 : low active 0 : high active	0
3:1	R	Reserved	-
0	R/W	HD Encoder Enable 1: Enable 0: Disable	0

Address : 0xF400_2804

Bit	R/W	Description	Default value
31:28	R	Reserved	-
27:16	R/W	Horizontal Back Porch Length [27:16] : Back Porch End Counter Value	0x104
15:12	R	Reserved	-
11:0	R/W	Horizontal High-level Sync Length [11:0] : Sync High End Counter Value	0x28

Address : 0xF400_2808

Bit	R/W	Description	Default value
31:28	R	Reserved	-
27:16	R/W	Horizontal Front Porch Length [27:16] : Front Porch End Counter Value	0x64a
15:12	R	Reserved	-
11:0	R/W	Horizontal Active Display Length [11:0] : Active Display End Counter Value	0x604

Address : 0xF400_280C

Bit	R/W	Description	Default value
31:12	R	Reserved	-
11:0	R/W	Horizontal Low-level Sync Length [11:0] : Sync Low End Counter Value	0x672

Address : 0xF400_2810

Bit	R/W	Description	Default value
31:27	R	Reserved	-
26:16	R/W	Vertical Back Porch Length [26:16] : Back Porch End Counter Value	0x19
15:11	R	Reserved	-
10:0	R/W	Vertical Sync Length [10:0] : Sync End Counter Value	0x5

Address : 0xF400_2814

Bit	R/W	Description	Default value
31:27	R	Reserved	-
26:16	R/W	Vertical Front Porch Length [26:16] : Front Porch End Counter Value	0x2ee
15:11	R	Reserved	-
10:0	R/W	Vertical Active Display Length [10:0] : Active Display End Counter Value	0x2e9

Address : 0xF400_2818

Bit	R/W	Description	Default value
31:22	R/W	Y Sync High-Base Level [31:22] : SyncHigh Level Value of dac input	0x22b
21	R	Reserved	-
20:11		Y Sync Base Level [20:11] : Sync Level Value of dac input	0x12b
10	R	Reserved	-
9:0	R/W	Y Sync Low-Base Level [9: 0] : Sync-Low Level Value of dac input	0x2b

Address : 0xF400_281C

Bit	R/W	Description	Default value
31:22	R/W	Pb,Pr Sync High-Base Level [31:22] : SyncHigh Level Value of dac input	0x255
21	R	Reserved	-
20:11		Pb,Pr Sync Base Level [20:11] : Sync Level Value of dac input	0x155
10	R	Reserved	-
9:0	R/W	Pb,Pr Sync Low-Base Level [9: 0] : Sync-Low Level Value of dac input	0x55

Address : 0xF400_2820

Bit	R/W	Description	Default value
31:26	R	Reserved	-
25:16	R/W	Color CbCr Offset [25:16] : Color Base Offset of dac sync sub input	0x40
15:10	R	Reserved	-
9:0	R/W	Luminance Offset [9: 0] : Lumin Base Offset of dac sync sub input	0x1b6

Address : 0xF400_2824

Bit	R/W	Description	Default value
31:16	R/W	HD DAC Color Level Calibration [27:16] : Fractional 12bit [31:28] : Integer 4bit	0xaab
15:0	R/W	HD DAC Luminance Level Calibration [11: 0] : Fractional 12bit [15:12] : Integer 4bit	0xae9

Address : 0xF400_2828

Bit	R/W	Description	Default value
31:18	R	Reserved	-
17:16	R/W	Color Pb,Pr Out Delay 00 : 0 Delay 01 : 3 Delay 10 : -3 Delay	0x0
15:2	R	Reserved	-
1:0	R/W	Luminance Y-Out Delay 00 : 0 Delay 01 : 3 Delay 10 : -3 Delay	0x0

20 Video Capture Engine

External Video input BT.656 format is saved as YcbCr or RGB format.

20.1 Features

- BT.656 Format decoding
- Support to capture YCbCr and load to memory
- Support to capture YcbCr and load to memory as RGB format(CSC mode)
  - Cutting the outline
  - Color conversion function (RGB565, RGB888)
- Capture one field function
- Capture one each two pixels
- Directly connected to Display controller

20.2 Register Description

20.2.1 Capture Control Register (CAPCTRL)

Address : 0xF400_2000

Bit	*R/W*	*Description*	*Default Value*
31:17	R	Reserved	-
16	R/W	Parity Check Enable 1: Parity Error Interrupt and Status Enable 0: Parity Check Disable	0
15	R/W	Select All Field Type on CSC Mode 1: Samples Odd, even field 0: Samples one between Odd or even field	0
14	R/W	Select Field Type on CSC Mode 1: Samples Even field 0: Samples Odd field	0
13	R/W	360pixels per 1 line on CSC Mode 1: load 360 pixel each line 0: load 720pixel each line	0
12	R/W	RGB888 on CSC Mode 1: RGB888 Conversion Mode 0: RGB565 Conversion Mode	0
11	R/W	CSC Enable 1: YCbCr to RGB Conversion Enable 0: Color Space Conversion Disable	0
10	R/W	Load to Memory Off 1: bypass to Display controller 0: load to memory	0
9:8	R	Reserved	-
7	R/W	Even field end Interrupt Enable 1: At the end of even field, interrupt is occurred. 0: Interrupt disable	0
6	R/W	Odd field end Interrupt Enable 1:At the end of Odd field, interrupt is occurred. 0: Interrupt disable	0
5	R/W	Capture Clock Inverting 1: Invert input clock 0: input clock	0
4	R/W	BT.656 Format Decoding Enable 1: BT.656 Format decoding 0: BT.656 Decoder disable	0
3:2	R/W	Select YCbCr Data Oder 3:2 L M 00: Y0 Cb0 Y1 Cr0 Y2 Cb1 Y3 Cr1 01: Y0 Cr0 Y1 Cb0 Y2 Cr1 Y3 Cb1 10: Cb0 Y0 Cr0 Y1 Cb1 Y2 Cr1 Y3 11: Cr0 Y0 Cb0 Y2 Cr1 Y2 Cb1 Y3	00
1	R/W	FIFO Read Request Level 1: Half Level 0: Quarter Level	0
0	R/W	ICE Enable 1: ICE Enable 0: ICE Disable	0

20.2.2 Capture Status Register (CAPSTS)

Address : 0xF400_2004

Bit	R/W	Description	Default value
31:5	R	Reserved	-
4	R	Even field end flag If completed, set, and It read, cleared	0
3:0	R	Reserved	-
0	R	Odd field end flag If completed, set, and It read, cleared	0

20.2.3 1st Odd Field Y/Cb/Cr Frame Buffer Address (YBUFADR0/ CbBUFADR0/CrBUFADR0)

Address : 0xF400_2008/0xF400_200C/0xF400_2010

Bit	R/W	Description	Default value
31:0	R/W	Odd Field 1st bank address	0

20.2.4 1st Even Field Y/Cb/Cr Frame Buffer Address (YBUFADR1/ CbBUFADR1/CrBUFADR1)

Address : 0xF400_2014/0xF400_2018/0xF400_201C

Bit	R/W	Description	Default value
31:0	R/W	Even Field 1st bank address	0

20.2.5 2nd Odd Field Y/Cb/Cr Frame Buffer Address (YBUFADR2/ CbBUFADR2/CrBUFADR2)

Address : 0xF400_2020/0xF400_2024/0xF400_2028

Bit	R/W	Description	Default value
31:0	R/W	Odd Field 2nd bank address	0

20.2.6 2nd Even Field Y/Cb/Cr Frame Buffer Address (YBUFADR3/ CbBUFADR3/CrBUFADR3)

Address : 0xF400_202C/0xF400_2030/0xF400_2034

Bit	R/W	Description	Default value
31:0	R/W	Even Field 2nd bank address	0

20.2.7 1st RGB Frame Buffer Address (FRAMEADR0)

Address : 0xF400_2008

Bit	R/W	Description	Default value
31:0	R/W	1st Bank address	0

20.2.8 2nd RGB Frame Buffer Address (FRAMEADR1)

Address : 0xF400_2014

Bit	R/W	Description	Default value
31:0	R/W	2nd Bank address	0

20.2.9 3rd RGB Frame Buffer Address (FRAMEADR2)

Address : 0xF400_2020

Bit	R/W	Description	Default value
31:0	R/W	3rd Bank address	0

20.2.10 4th RGB Frame Buffer Address (FRAMEADR3)

Address : 0xF400_202C

Bit	R/W	Description	Default value
31:0	R/W	4-thBank address	0

20.2.11 Display Offset (OFFSET)

Address : 0xF400_2038

Bit	R/W	Description	Default Value
31:0	R/W	In CSC Mode line, The number of pixel is to next line	0

20.2.12 Number of Upper Line to Cut (NUMLINECUT0)

Address : 0xF400_203C

Bit	R/W	Description	Default Value
31:0	R/W	In the CSC Mode, the number of upper line is not displayed	0

20.2.13 Number of Lower Line to Cut (NUMLINECUT1)

Address : 0xF400_2040

Bit	R/W	Description	Default Value
31:0	R/W	In the CSC Mode, the number of lower line is not displayed	0

20.2.14 Number of Left Pixel to Cut (NUMPXLCUT0)

Address : 0xF400_2044

Bit	R/W	Description	Default Value
31:0	R/W	In CSC Mode, the number of left-hand pixel is not displayed	0

20.2.15 Number of Right Pixel to Cut (NUMPXLCUT1)

Address : 0xF400_2048

Bit	R/W	Description	Default Value
31:0	R/W	In CSC Mode, the number of right-hand pixel is not displayed	0

20.2.16 Display Output Width (OUTPUTWIDTH)

Address : 0xF400_204C

Bit	R/W	Description	Default Value
31:0	R/W	In CSC Mode, the number of total line pixel used by display controller is displayed. next line is start address.	0

21 Graphics Engine

21.1 Features

- 14 Stage (including Alpha Blend procedure) Pipe Line Processing
- Supports 2048 * 2048 (Max) Resolution
- Supports 2048 * 2048 (Max) Texture Size

21.1.1 Rendering Procedure

- Supports Tile Addressing Mode
- Internal true color processing
- Supports 24bpp with Alpha/16bpp / 8bpp / 4bpp texel
  - (Using palette memory (256*24bit) @ 8bpp or 4bpp texel mode)
- Supports Various Pixel Format
  - ARGB, RGBA, ABGR, BGRA

- Texture Mapping (Zoom in / Zoom out / Rotation /Clipping)
- Flat Shading
- Alpha Blending with Blending functions(OpenGL Compatible with out saturate alpha mode)
  - One, Zero, Destination color, 1-Destination color, Source color, 1-Source color
  - Source alpha, 1-source alpha, Destination Alpha, 1-Destinaiton Alpha, Constant color
  - 1-Constant color, Constant Alpha, 1-Constant Alpha

- Transparent Pixel Processing
- Dithering (2*2 or 4*4)
- Mosaic (2*2, 4*4, 8*8, 16*16, 32*32, 16*32, 16*32)

21.1.2 *Rasterization Procedure*

Adopt OpenGL's Double Buffer Architecture
Pixel Color Depth : 16bit (RGB 5/6/5) or 32bit (ARGB)

21.2 Block Diagram

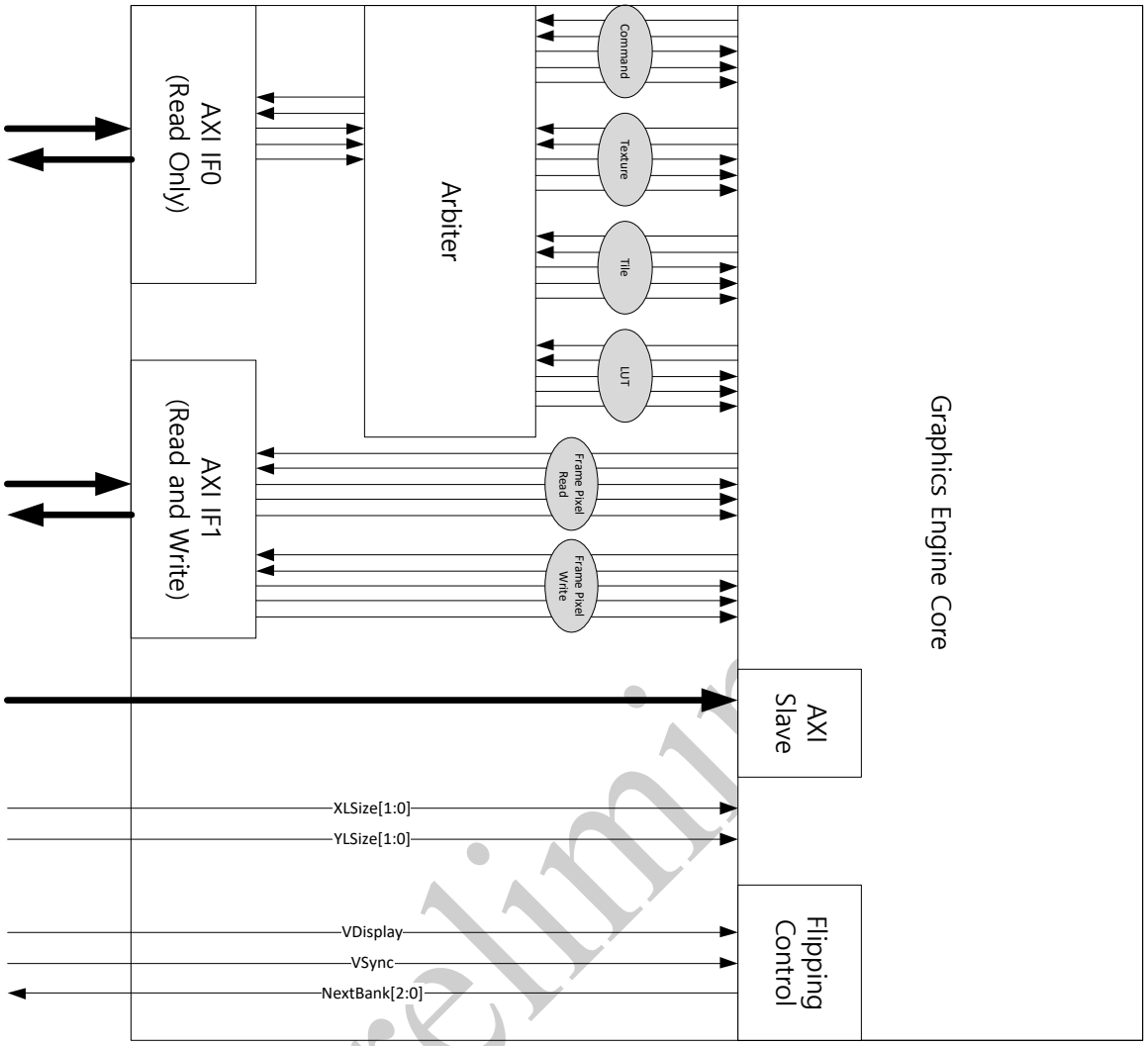


Figure 21-1 Graphics Engine Block Diagram

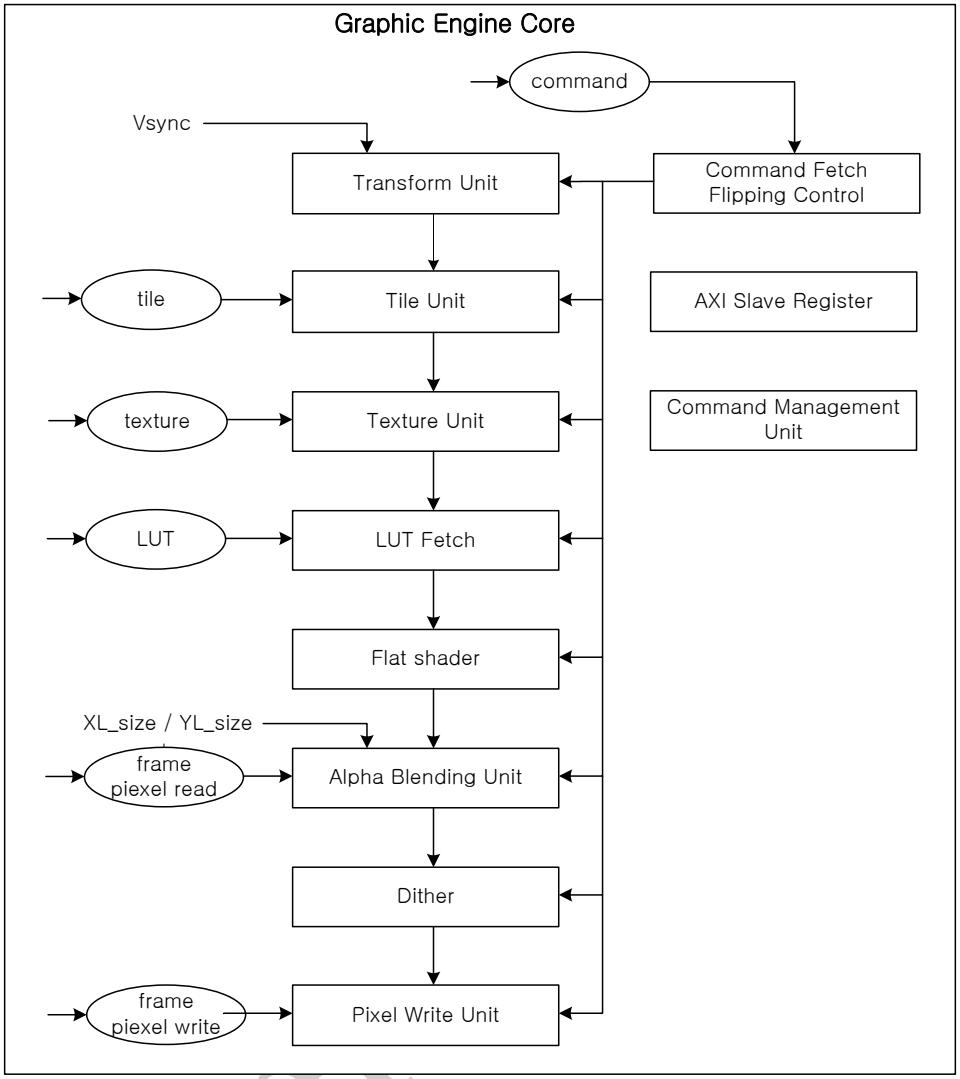


Figure 21-2 Graphics Engine Core Block Diagram

21.3 Graphics Engine Command Format

Table 21-1 Graphics Engine Command Format

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Etc.			**Texture Mapping & Effect Command**									**Flipping Command**			
PD[0]		32Bit Frame Buffer Format	Palette Update	Mosaic Mode 3'b000: Disable 3'b100: 16*16 3'b001:2*2 3'b101: 32*32 3'b010: 4*4 3'b110: 32*16 3'b011: 8*8 3'b111: 16*32			Alpha Enable	Shade / Light Enable	Trans Enable	Clipping Enable	Tile Mode	Texture Mapping Enable			Sync Flip	Async Flip
PD[1]										E6	E5	E4	E3	E2	E1	E0
Group#0 (Display Area Parameter)																
PD[2]						Dx[10:0]										
PD[3]						Dy[10:0]										
PD[4]						EndDx[10:0]										
PD[5]						EndDy[10:0]										
Group#1 (Texture start point S.11.9 [sign,integer 11bit,fractional 9bit] signed 2's complement format)																
PD[6]	Tx[15:0]															
PD[7]												Tx[20:16]				
PD[8]	Ty[15:0]															
PD[9]												Ty[20:16]				
Group#2 (Texture deviation according to display increment S.11.9 [sign,integer 11bit,fractional 9bit] signed 2's complement format)																
PD[10]	DTxdx[15:0]															
PD[11]												DTxdx[20:16]				
PD[12]	DTydx[15:0]															
PD[13]												DTydx[20:16]				
PD[14]	DTxdy[15:0]															
PD[15]												DTxdy[20:16]				
PD[16]	DTydy[15:0]															
PD[17]												DTydy[20:16]				
Group#3 (Alpha Parameter)																
PD[18]	Constant Color[15:0] (G,B)															
PD[19]	Constant Color[31:24] (Alpha)								Constant Color[23:16] (R)							
PD[20]					Dest Blend value Inversion	Dest Blend Function 3'b000:Zero 3'b001:Constant 3'b010:Source Alpha 3'b011:Source Pixel 3'b100:Dest Alpha 3'b101:Dest Pixel						alpha 1 round error correction	Source Blend value Inversion	Source Blend Function 3'b000:Zero 3'b001:Constant 3'b010:Source Alpha 3'b011:Source Pixel 3'b100:Dest Alpha 3'b101:Dest Pixel		
Group#4 (Color Gain Parameter. For Shading or Lighting Effect)																
PD[21]														Shade Color Gain 3'bxx1:Light Blue Enable 3'bx1x:Light Green Enable 3'b1xx:Light Red Enable		
PD[22]	Shade Color[15:0] (G,B)															
PD[23]	Shade Color[31:24] (Alpha)								Shade Color[23:16] (R)							
Group#5 (Transparent Parameter)																
PD[24]	Transparent Color[15:0] (G,B)															
PD[25]									Transparent Color[23:16] (R)							
Group#6 (Address Offset & Etc..)																
PD[26]	Tile Offset[21:6]															
PD[27]											Tile Offset[27:22]					
PD[28]	Font Offset[21:6]															
PD[29]											Font Offset[27:22]					
PD[30]	Palette Offset[27:12]															
PD[31]	Palette Bank Select This Parameter used only @ 4bpp Texel mode					Texel Format 3'b000: 4bpp 3'b001: 8bpp 3'b010: 16bpp 3'b100: 32bpp(ARGB) 3'b101: 32bpp(ABGR) 3'b110: 32bpp(RGBA) 3'b111: 32bpp(BGRA)			Texture (Tile) Height Log_2(Height) -3				Texture (Tile) Width Log_2(Height) -3			
						Texture Real Width(2047~0)										
						Texture Data Stride(2047~0)										
						Texture Height (2047~0)										

21.4 Register Description

21.4.1 Command Packet Write Pointer Register

Address : 0x8000_0000

Bit	R/W	Description	Default value
31:16	R	Reserved	-
10: 0	R/W	Command packet Write pointer cleared at the completion of the engine	

21.4.2 Command Packet Read Pointer Register

Address : 0x8000_0004

Bit	R/W	Description	Default value
31:16	R	Reserved	-
10: 0	R/W	Command packet Read pointer 1. This value is increased after reading current command packet. When the engine becomes inactive, this bit is reset to '0'. 2. This value is set when the engine is in inactive state.	

21.4.3 Rendering Control Register

Address : 0x8000_0008

Bit	R/W	Description	Default value
31:16	R	Reserved	-
8	R/W	"EndRender" Write FIFO Flush Enable (Whenever Packet processing Finished, FIFO Flush operation proceed) 0: Disable EndRender Flush Operation. 1: Enable EndRender Flush Operation.	0
7 : 6	R/W	Dithering mode 00 : disable. 01 : 2X2 dithering 1X : 4X4 dithering	00
5 : 2		Reserved	
0	R/W	Engine Enable	00

21.4.4 Current Bank Register

Address : 0x8000_000C

Bit	R/W	Description	Default value
31:16	R	Reserved	-
24	R	Rendering Engine Idle Status 0 : Busy Status 1: Idle Status	1
23:18		Reserved	0
17:16		Reserved	0
15: 0		Reserved	0
9 : 8	R/W	Asynchronous Flip Bank	00
7 : 2		Reserved	0
1 : 0	R	Current Display Bank	00

21.4.5 Flip Command Register

Address : 0x8000_0010

Bit	R/W	Description	Default value
31:16	R	Reserved	-
7 : 0	R/W	Flip Command Count Write "0" : Reset count value Write "1" : increase count value by "1 " When flipping Command executes, this value decreases by "1"	0x00

21.4.6 Texture Base Address Register

Address : 0x8000_0014

Bit	R/W	Description	Default value
31:20	R/W	Texture Base Address[31:20]	0
19: 0	R	Reserved	

21.4.7 Frame Base Address0 Register

Address : 0x8000_0018

Bit	R/W	Description	Default value
31:20	R/W	Frame Base Address[31:16]	0
15: 0	R	Reserved	

21.4.8 Frame Base Address1 Register

Address : 0x8000_001C

Bit	R/W	Description	Default value
31:20	R/W	Frame Base Address[31:16]	0
15: 0	R	Reserved	

21.4.9 Frame Base Address2 Register

Address : 0x8000_0020

Bit	R/W	Description	Default value
31:20	R/W	Frame Base Address[31:16]	0
15: 0	R	Reserved	

21.4.10 Frame Base Address3 Register

Address : 0x8000_0024

Bit	R/W	Description	Default value
31:20	R/W	Frame Base Address[31:16]	0
15: 0	R	Reserved	

21.4.11 Current Rendering Base Address Register

Address : 0x8000_0024

Bit	R/W	Description	Default value
31:20	R/W	Current Rendering Base Address[31:16]	0
15: 0	R	Reserved	

22 JPEG Decoder

22.1 Features

- Available within 35ms for decoding 640x480 4:2:0 format 1frame(Lena image)
- ISO 10918-2 base line JPEG decoder
- Only support typical Huffman table defined in annex K of standard.
- Support YCbCr 4:2:2 format
- Support YCbCr 4:2:0 format
- Maximum resolution:2048x2048

22.2 Block Description

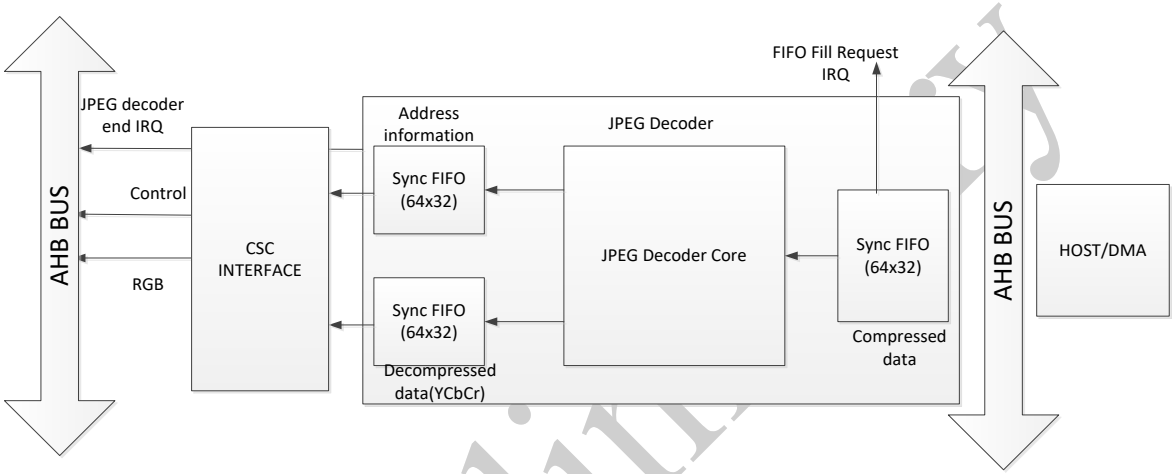


Figure 22-1 JPEG Decoder Block Diagram

There are three 64x32 FIFOs in JPEG Decoder for storing JPEG Image data, decompressed DATA (YCbCr) and address informant of MCU(Minimum Code Unit). The FIFO's level is decided by setting value of JDFCON Register[6:0].

During the operation of JPEG decoder, FIFO Fill Request IRQ (Level Trigger) is triggered in decoder by JPEG Image data Request. IRQ is held when data fills the FIFO up to the FIFO level set in JDCTRL register and cleared automatically when the number of DATA in FIFO is more than the level of FIFO. IRQ reoccurs when number of data in FIFO is below the FIFO level.

JPEG Decoder ends the IRQ that indicates end of image decoding when JPEG Image EOI (End Of Image) Maker is decoded. This IRQ is an Interrupt source of JPEG Image Capturer, and JPEG Image Capturer uses this interrupt source to generate JPEG Image Capture IRQ (JICCIRQ) when the last MCU data is stored into Memory. JICIRQ is held until user clears the JPEG Decoder End IRQ by software.

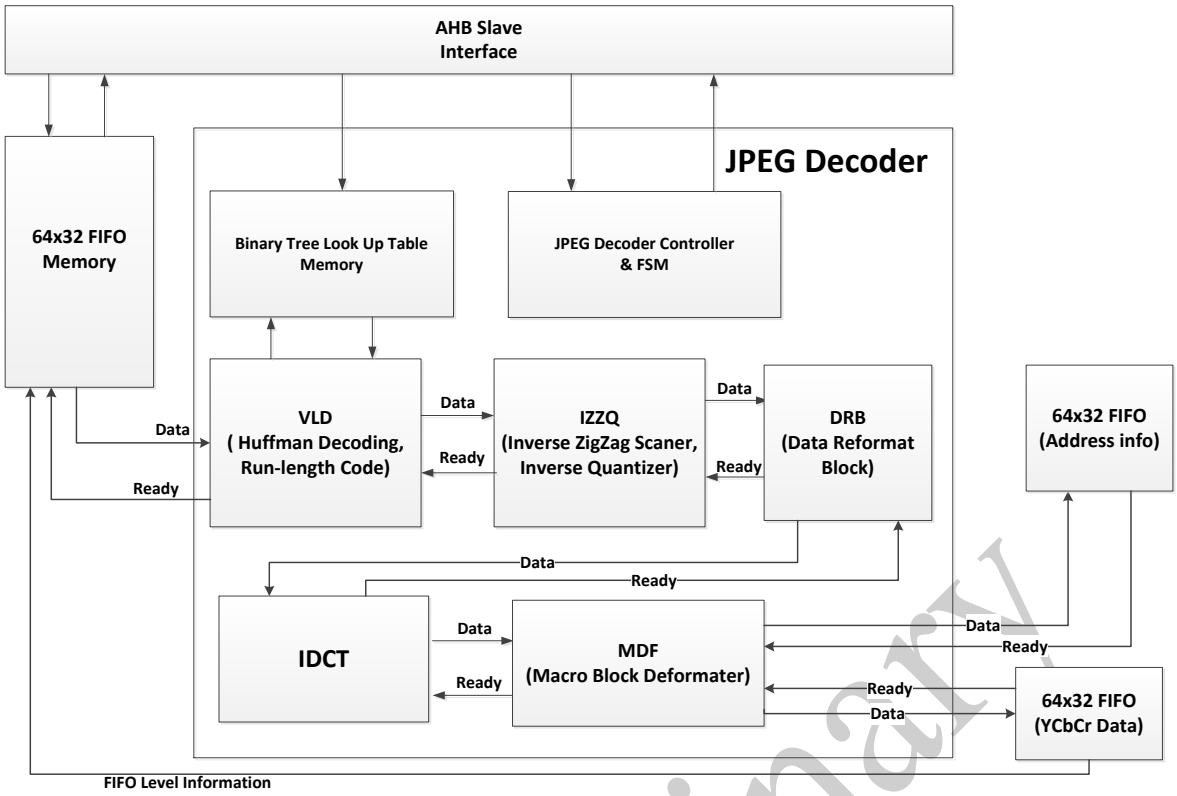
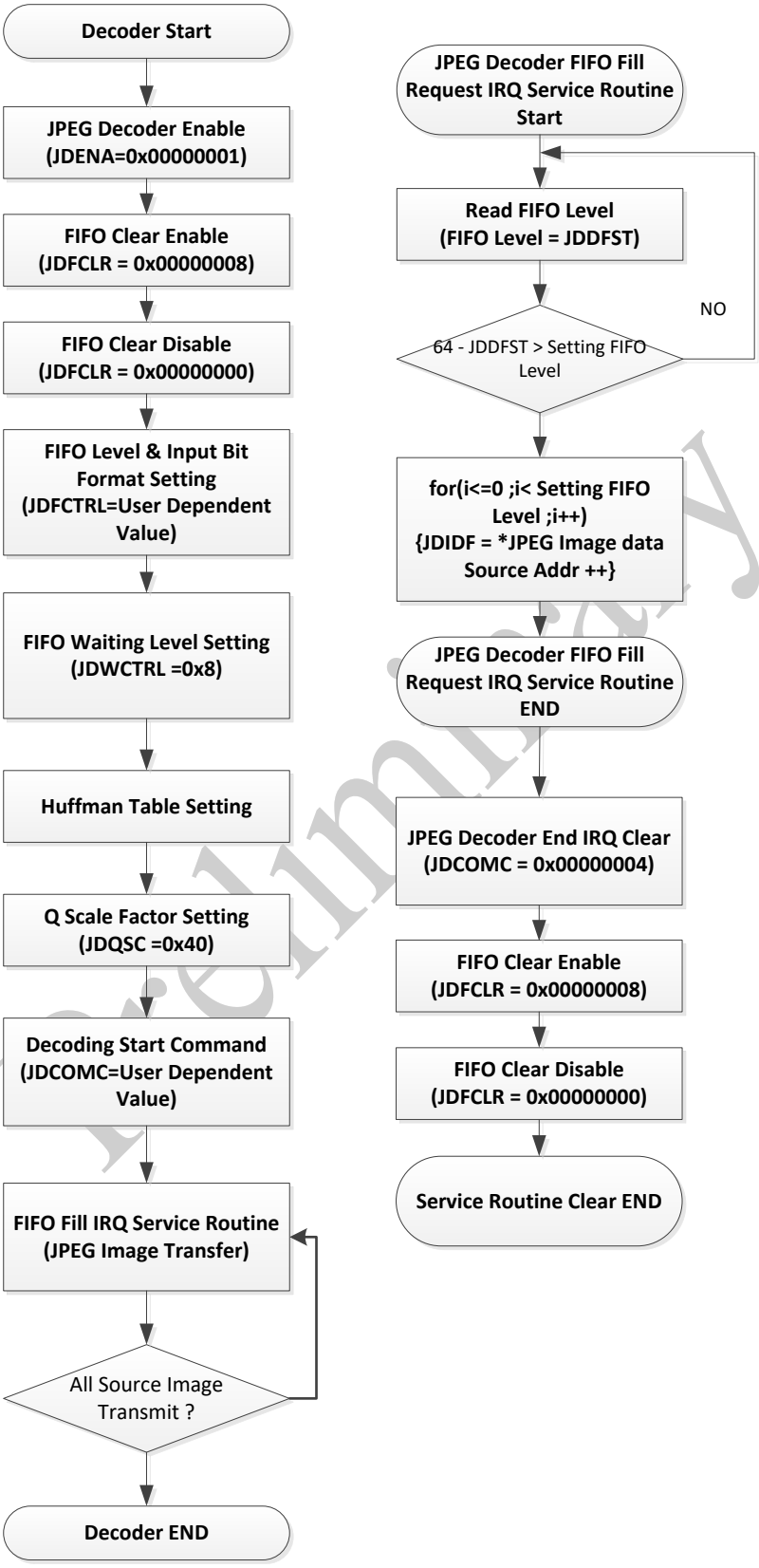


Figure 22-2 Decoder Core Block Diagram

Each JPEG Decoder block transmit data output to the next stage operation block based on ready signal generated by the next stage operation block. JPEG enters waiting state when a JPEG image input stream is waiting due to external system condition or output data is filling the FIFO up to the level set in JDWCON register. JPEG Decoder is restarted from the waiting point, when Input Image stream is resumed or numbers of output data in FIFO is below the programmed FIFO level.

22.3 Function Description



22.4 Register Description

22.4.1 JPEG Decoder Quantization Scale Control Register (JDQSC)

Address: 0xF001_023C

Bit	R/W	Description	Default value
31 : 12	R	Reserved.	
11 : 0	W	JPEG Quantization Scale Control Scale quantization table value in the JPEG image header. With 64 as base value, larger number increases Q table value and smaller number decreases Q table value If other value other than 64 is used, image distortion may occur under the condition of different value setting.	000h

22.4.2 JPEG Decoder Command Control Register (JDCOMCON)

Address: 0xF001_0240

Bit	R/W	Description	Default value
31 : 3	R	Reserved.	
2	W	JPEG Decoder End IRQ Clear 1:End IRQ Clear 0:IDLE JPEG Decoder End IRQ is used as JICIRQ source. This bit is set when both JPEG Decoder End IRQ and JICIRQ are cleared. After changing to '1', this bit will toggle back to '0' at the next clock. After this bit is set to '1', it is automatically cleared to '0' at the next clock. *JPEG Decoder End IRQ must be cleared for JPEG decoder to decode the next image	0b
1	W	DECODING IMAGE FORMAT 1:YCBCR 420 0:YCBCR 422	0b
0	W	Decoding Start 1:Decoding Start 0:IDLE If JDENA Register[0] is set to '1', JPEG decoder shall operate when this bit changes to '1'. The first JPEG Decoder FIFO Fill Request IRQ is initiated by setting this bit to '1'. After decoder starts the decoding operation, this bit will be cleared automatically.	0b

22.4.3 JPEG Decoder Y dc node Table (JDYDCNT)

Address: 0xF001 0800 ~ F001 0830

Bit	R/W	Description	Default value
31 : 12	R	Reserved.	
17 : 0	W	Y DC Node Table for Huffman Decoding The node table of Y DC binary tree used for Huffman decoding	000h

22.4.4 JPEG DECODER Y DC LEAF Table (JDYDCLT)

Address : 0xF001 0C00 ~ F001 0C30

Bit	R/W	Description	Default value
31 : 8	R	Reserved	-
7 : 0	W	Y DC LEAF Table for Huffman Decoding The leaf table of Y DC binary tree used for Huffman decoding	-

22.4.5 JPEG DECODER Y AC NODE Table (JDYACNT)

Address : 0xF001 2800 ~ F001 2A88

Bit	R/W	Description	Default value
31 : 18	R	Reserved	-
17 : 0	W	Y AC Node Table for Huffman Decoding The node table of Y AC binary tree used for Huffman decoding	-

22.4.6 JPEG DECODER Y AC LEAF Table (JDYACLT)

Address : 0xF001 3000 ~ F001 3288

Bit	R/W	Description	Default value
31 : 8	R	Reserved	-
7 : 0	W	Y AC LEAF Table for Huffman Decoding The leaf table of Y AC binary tree used for Huffman decoding	-

22.4.7 JPEG DECODER UV DC NODE Table (JDUVDCNT)

Address : 0xF001 4800 ~ F001 4830

Bit	R/W	Description	Default value
31 : 18	R	Reserved	-
17 : 0	W	UV AC Node Table for Huffman Decoding The node table of UV DC binary tree used for Huffman decoding	-

22.4.8 JPEG DECODER UV DC LEAF Table (JDUVDCLT)

Address : 0xF001 5000 ~ F001 5030

Bit	R/W	Description	Default value
31 : 8	R	Reserved	-
7 : 0	W	UV DC LEAF Table for Huffman Decoding The leaf table of UV DC binary tree used for Huffman decoding	-

22.4.9 JPEG DECODER UV AC NODE Table (JDUVACNT)

Address : 0xF001 6800 ~ F001 6A88

Bit	R/W	Description	Default value
31 : 18	R	Reserved	-
17 : 0	W	UV AC Node Table for Huffman Decoding The node table of UV AC binary tree used for Huffman decoding	-

22.4.10 JPEG DECODER UV AC LEAF Table (JDUVACLT)

Address : 0xF001 7000 ~ F001 7288

Bit	R/W	Description	Default value
31 : 8	R	Reserved	-
7 : 0	W	UV AC LEAF Table for Huffman Decoding The leaf table of UV AC binary tree used for Huffman decoding	-

22.4.11 JPEG DECODER STATUS Register (JDSTAT)

Address : 0xF001 8000

Bit	R/W	Description	Default value
31 : 4	R	Reserved	-
3	R	JPEG Decoder Finished	0b
2	R	JPEG Decoder MCU Decoding	0b
1	R	JPEG Decoder Header Parsing	0b
0	R	JPEG Decoder Ready	0b

22.4.12 JPEG DECODER IRQ STATUS Register (JDIRQSTAT)

Address : 0xF001 8004

Bit	R/W	Description	Default value
31 : 2	R	Reserved.	-
2	R	JPEG Decoder Timeout Interrupt is generated when a time-out value is reached due to an abnormal function or compressed input data failure for some time. Even if terminated by time-out, software reset and the interrupt clearing processed to resume to initial state.	0b
1	R	JPEG Decoder FIFO Fill Request IRQ Interrupt is triggered when the compressed data in JPEG Decoder Internal FIFO is not filled up to the level configured in JDCTRL Register [6:0].	0b
0	R	JPEG Decoder End IRQ Display the end point of JEPG Decoder. after JPEG Decoder decodes the required number of MCU in decoder, this IRQ shall occur when JPEG EOF Flag is arrives in Decoder. *this interrupt is inputted to JPEG image capturer and used for the source of JICIRQ.	0b

22.4.13 JPEG DECODER Data FIFO Status Register (JDDFSTAT)

Address : 0xF001 8008

Bit	R/W	Description	Default value
31 : 7	R	Reserved.	-
6 : 0	R	Current FIFO Level Status Show current input data FIFO level. When input data is written into the FIFO, input data must be written within the value of Current FIFO Level Status of under 3Fh. If exceeded, new subsequent data will overwrite the existing data in FIFO.	00h

22.4.14 JPEG DECODER Enable Register (JDENA)

Address : 0xF001 8010

Bit	R/W	Description	Default value
31 : 1	R	Reserved.	-
0	R/W	JPEG Decoder Enable This bit enables JPEG decoder. After this bit is set to 1, JPEG Decoder shall start data decoding when bit 0 of JDCOMCON register is set to '1'.	0b

22.4.15 JPEG DECODER FIFO Clear Register (JDFCLR)

Address : 0xF001 8014

Bit	R/W	Description	Default value
31: 4	R	Reserved.	-
3	R/W	FIFO Clear 1:ALL FIFO Clear 0:IDLE	0b
2 : 0	R	Reserved	-

22.4.16 JPEG DECODER FIFO Control Register (JDFCON)

Address : 0xF001 8018

Bit	R/W	Description	Default value
31 : 10	R	Reserved	-
9	R/W	Input data Format Selection 1:Big Endian Format 0:Little Endian Format	0b
7 : 8	R	Reserved	-
6 : 0	R/W	Data FIFO Threshold Level This field identifies the threshold level of data FIFO. FIFO Fill Request Interrupt occurs when number of data into FIFO is below the value set in this field. lower value must be used for setting values other than FIFO size(64)	00h

22.4.17 JPEG DECODER WAITE CONTROL Register (JDWCON)

Address : 0xF001 801C

Bit	R/W	Description	Default value
31 : 7	R	Reserved	-
6 : 0	R	WAITE FIFO Threshold Level This field determines the decoding data output FIFO level. Decoder goes into waiting mode when the number of data stored in FIFO is 8 times the WAITE FIFO Threshold Level value and operates again when the remaining data in FIFO is below the value of WAITE FIFO Threshold Level *8 The value range is between a minimum 1 to a maximum 8, the smaller the value, the more frequent the decoder has to wait.	08h

22.4.18 JPEG DECODER SOFTWARE RESET Register (JDSRST)

Address : 0xF001 8024

Bit	R/W	Description	Default value
31 : 1	R	Reserved.	-
0	R/W	Software Reset 1:IDLE 0:Reset This bit forces a decoder initialization when JPEG decoder is not operating under normal condition by taking in wrong data. The decoder shall enter reset state when this bit is set to '0', and operation starts again when this bit is set to '1'.	1b

22.4.19 JPEG DECODER Version Information Register (JDVERINFO)

Address : 0xF001 8028

Bit	R/W	Description	Default value
31 : 0	R/W	JPEG Decoder Version	-

22.4.20 JPEG DECODER CSC Base Address Register (JDCSCBASEADDR)

Address : 0xF001 802C

Bit	R/W	Description	Default value
31 : 0	R/W	JPEG Decoder RGB data Base address for transferring	C2000000h

22.4.21 JPEG DECODER CSC Base Address Register (JDCSTRID)

Address : 0xF001 8030

Bit	R/W	Description	Default value
31 : 0	R/W	JPEG Decoder Stride size	400h

22.4.22 JPEG DECODER RGB565 mode and Timeout count enable (JDCRGBTIMEOUT)

Address : 0xF001 8034

Bit	R/W	Description	Default value
0	R/W	JPEG Decoder RGB888/565 mode 0 : RGB888 mode 1 : RGB565 mode	0h
1	R/W	JPEG Decoder timeout counter ctrl 0 : disable Timeout counter 1 : enable Timeout counter	0h

22.4.23 JPEG DECODER Timeout counter Register (JDCTIMEOUTCNT)

Address : 0xF001 8038

Bit	R/W	Description	Default value
31 : 0	R/W	JPEG Decoder timeout counter register When JPEG abnormally stop due to corrupted data input, time-out is detected with time-out value.	8000000h

22.4.24 JPEG DECODER Timeout counter clear (JDCTIMEOUTCLR)

Address : 0xF001 8038

Bit	R/W	Description	Default value
0	R/W	JPEG Decoder timeout counter clear register When timer-out is occurred, it must be cleared by this bit to continue to run. 1 : timeout clear set 0 : timeout clear off	0h

22.4.25 JPEG DECODER INPUT DATA FIFO Register (JDIDF)

Address : 0xF001 9000

Bit	R/W	Description	Default value
31 : 0	W	INPUT DATA FIFO Compressed data(JPEG Input stream) FIFO	-

23 Sound Mixer

23.1 Features

- 4-CH. Player, 1-CH Recorder
- Re-Sampler
- Gain Controller
- 32-Depth Buffer for each channel
- 1 Out (I2S)

23.2 Block Diagram

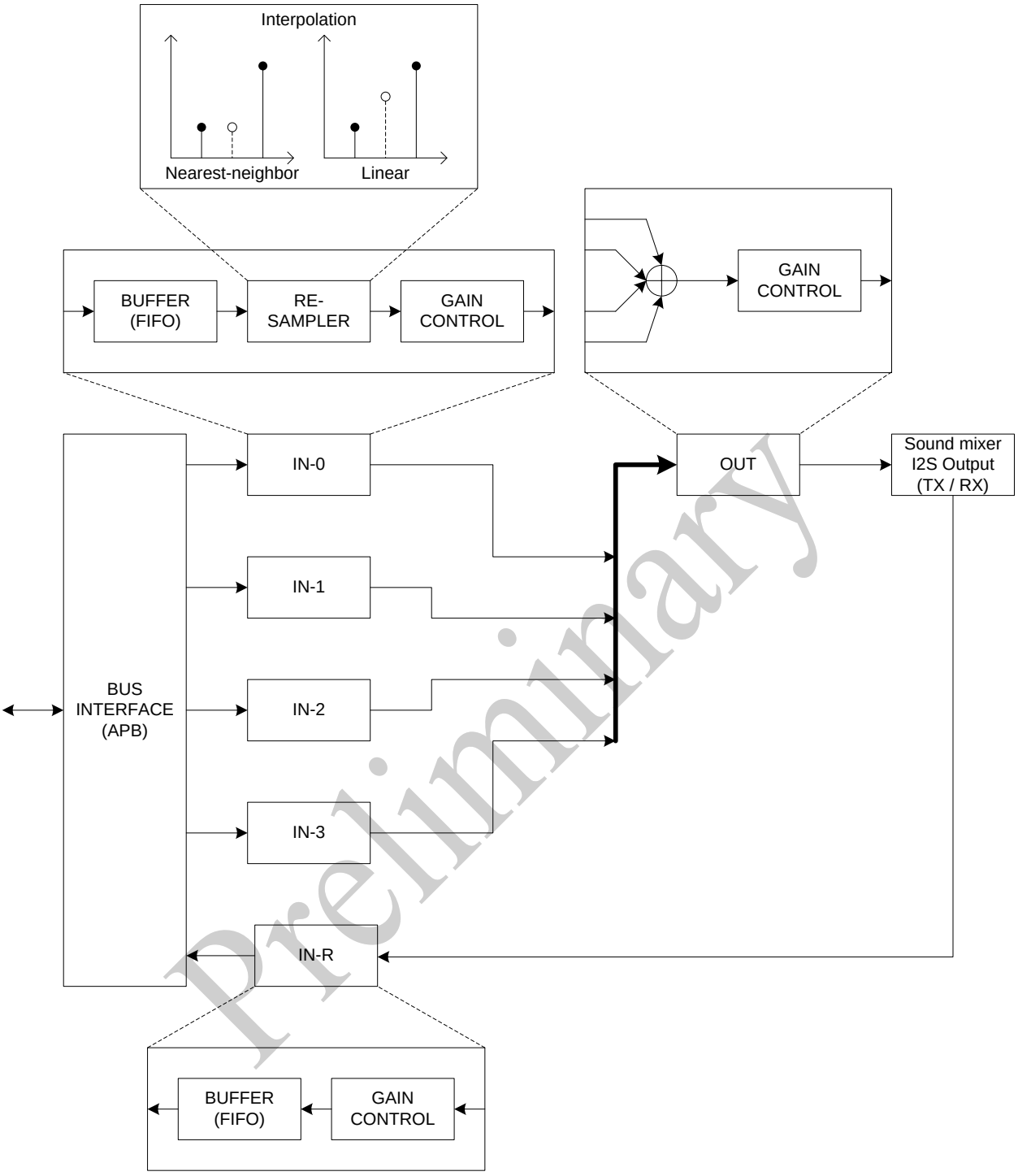


Figure 23-1 Mixer Block Diagram

23.3 Sound Mixer I2S Output Frequency Control

SCLK, LRCK, and MCLK frequency should be configured to use I2S output. Following table shows the relationship between MCLK and LRCK. For example, if master frequency is set 256fs for 44.1kHz, MCLK should be set 11.2896MHz. The corresponding MCLK can be configured by using pre-scaler.

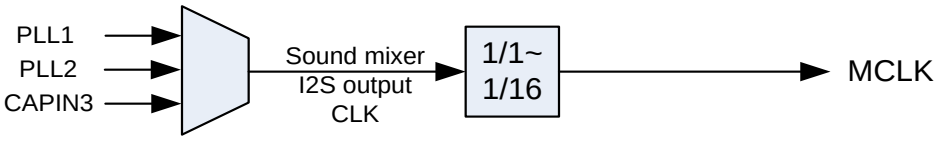


Figure 23-2 MCLK Pre-Scaler

Table 23-1 I2S Sampling Frequency(LRCK) and MCLK Clock

LRCK (fs)	***8.000 KHz***	***11.025 KHz***	***16.000 KHz***	***32.000 KHz***	***44.100 KHz***	***48.000 KHz***	***96.000 KHz***
MCLK (MHz)	256fs						
	2.048	2.8224	4.096	8.1920	11.2896	12.2880	24.5760
	384fs						
	3.072	4.2336	6.144	12.2880	16.9344	18.4320	36.8640
	512fs						
	4.096	5.6448	8.192	16.3840	22.5792	24.5760	49.1520

Also, following table shows SCLK configuration

Table 23-2 Sound Mixer I2S Output sampling frequency and serial bit clock

Serial bit per channel	***8bit***	***16bit***
CODEC Clock(MCLK)	Serial clock frequency(SCLK)	
256fs	16fs, 32fs, 64fs	32fs, 64fs
384fs	16fs, 32fs, 48fs, 64fs	32fs, 48fs, 64fs
512fs	16fs, 32fs, 64fs	32fs, 64fs

23.4 Register Description

23.4.1 Mixer Control Register (MIXER_ CON)

Address: 0xF400_5000, 0xF400_5010, 0xF400_5020, 0xF400_5030 (IN-0, IN-1, IN-2, IN-3)

Bit	*R/W*	*Description*	*Default Value*
31 : 29	R	Reserved	-
28	R/W	Method of interpolation 0: Nearest-neighbor 1: Linear	0x0
27 : 25	R	Reserved	-
24 : 16	R/W	Step for re-sampling N = ((InFs * 256) / OutFs) – 1, (N=0~511)	0x0FF
15 : 10	R	Reserved	-
9 : 8	R/W	Out selection 00: Out-0 : (This valued must be used)	0x00
7 : 4	R/W	Mode 0000: Unsigned stereo 8-bit PCM 0001: Unsigned mono 8-bit PCM 0010: Signed stereo 8-bit PCM 0011: Signed mono 8-bit PCM 0100: Unsigned stereo 16-bit PCM 0101: Unsigned mono 16-bit PCM 0110: Signed stereo 16-bit PCM 0111: Signed mono 16-bit PCM 1xxx: Reserved	0x0
3	R/W	DMA request 0: Disable 1: Enable	0x0
2	R/W	Interrupt 0: Disable 1: Enable	0x0
1	R/W	L/R swap 0: Disable 1: Enable	0x0
0	R/W	Active 0: Disable 1: Enable	0x0

Address: 0xF400_5070 (IN-R)

Bit	R/W	Description	Default Value
31 : 2	R	Reserved	-
3	R/W	DMA request 0: Disable 1: Enable	0x0
2	R/W	Interrupt 0: Disable 1: Enable	0x0
1	R/W	Reserved	-
0	R/W	Active 0: Disable 1: Enable	0x0

Address: 0xF400_5080 (OUT-0)

Bit	R/W	Description	Default Value
31 : 1	R	Reserved	-
0	R/W	Active 0: Disable 1: Enable	0x0

23.4.2 Mixer Volume Register (MIXER_VOL)

Address: 0xF400_5004, 0xF400_5014, 0xF400_5024, 0xF400_5034, 0xF400_5074, 0xF400_5084
(IN-0 ~ IN-3, IN-R, OUT-0)

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	-
15 : 8	R/W	Right gain (±0.5dB) 0xFF(0dB) ~ 0x80(-63.5dB), 0x7F~0x0(-∞dB)	0xFF
7 : 0	R/W	Left gain (±0.5dB) 0xFF(0dB) ~ 0x80(-63.5dB), 0x7F~0x0(-∞dB)	0xFF

23.4.3 Mixer Buffer Status Register (MIXER_BST)

Address: 0xF400_5008, 0xF400_5018, 0xF400_5028, 0xF400_5038, 0xF400_5078
(IN-0 ~ IN-3, IN-R)

Bit	R/W	Description	Default Value
31 : 6	R	Reserved	-
5 : 0	R	Buffer count value 0(Empty) ~ 32(Full)	0x0

23.4.4 Mixer Data Register (MIXER_DAT)

Address: 0xF400_500C, 0xF400_501C, 0xF400_502C, 0xF400_503C, 0xF400_507C
(IN-0 ~ IN-3, IN-R)

Bit	R/W	Description	Default Value
31 : 0	R/W	PCM data	-

23.4.5 Mixer Out Register (MIXER_OUT)

Address: 0xF400_508C (OUT-0)

Bit	R/W	Description	Default Value
31 : 6	R/W	Reserved	-
15	R/W	Presclaer Enable bit 0 : Disabled 1 : Enabled	
14 : 13	R	Reserved	
12 : 8	R/W	Prescaler divider value 00000 : 1 00001 : 2 00002 : 3 ~ 11111 : 32	
7 : 6	R	Reserved	
5	R/W	Left of LRCK signal 0: High 1: Low	0x0
4	R/W	Format 0: I2S-bus 1: MSB(Left)-justified	0x0
3 : 2	R/W	MCLK frequency 00: 256fs 01: 384fs 10: 512fs 11: Reserved	0x0
1 : 0	R/W	SCLK frequency 00: 16fs 01: 32fs 10: 48fs 11: 64fs	0x0

23.4.6 Mixer Interrupt Status Register (MIX_IST)

Address: 0xF400_50C0

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	R	IN-R interrupt	0x0
6 : 4	R	Reserved	-
3	R	IN-3 interrupt	0x0
2	R	IN-2 interrupt	0x0
1	R	IN-1 interrupt	0x0
0	R	IN-0 interrupt	0x0

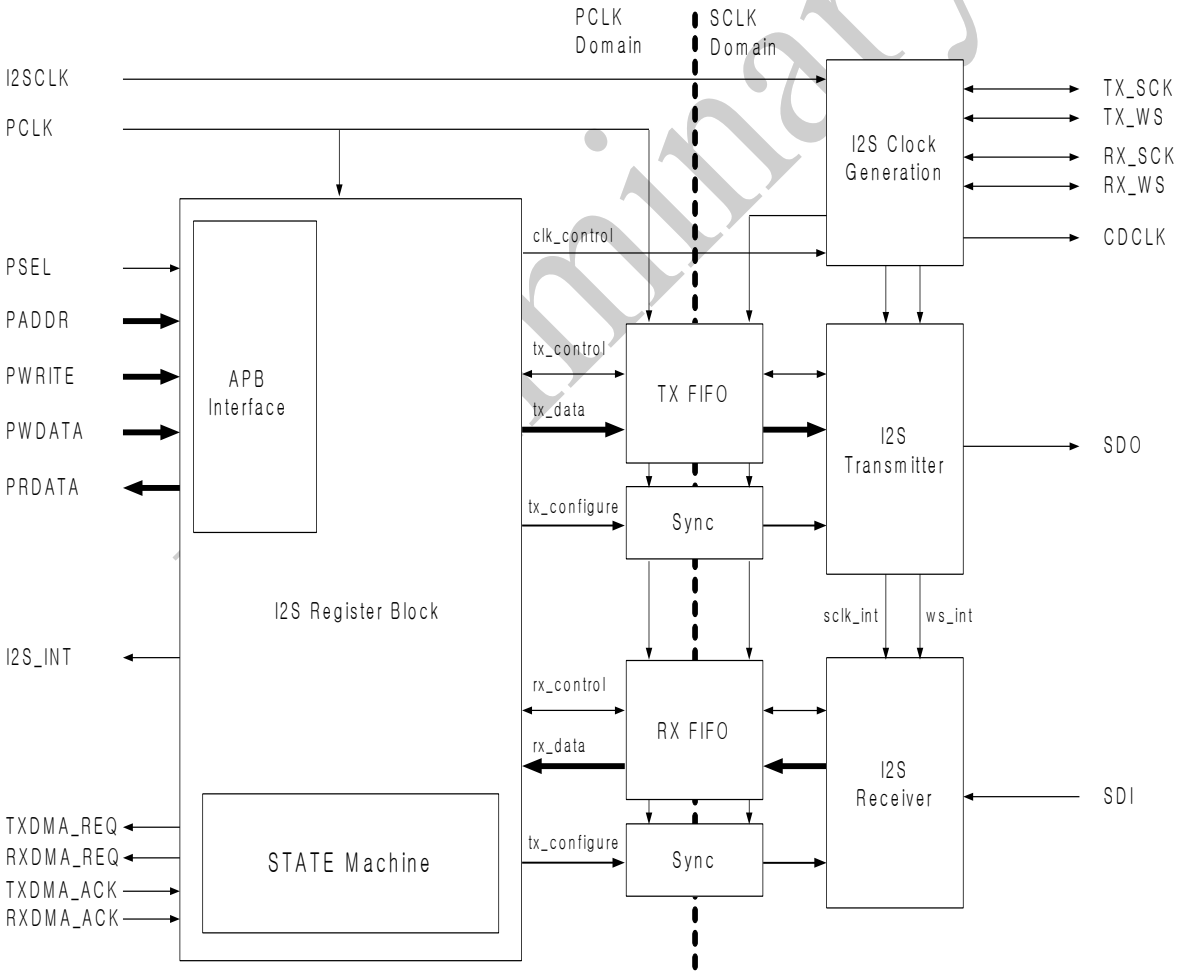
24 I2S

24.1 Features

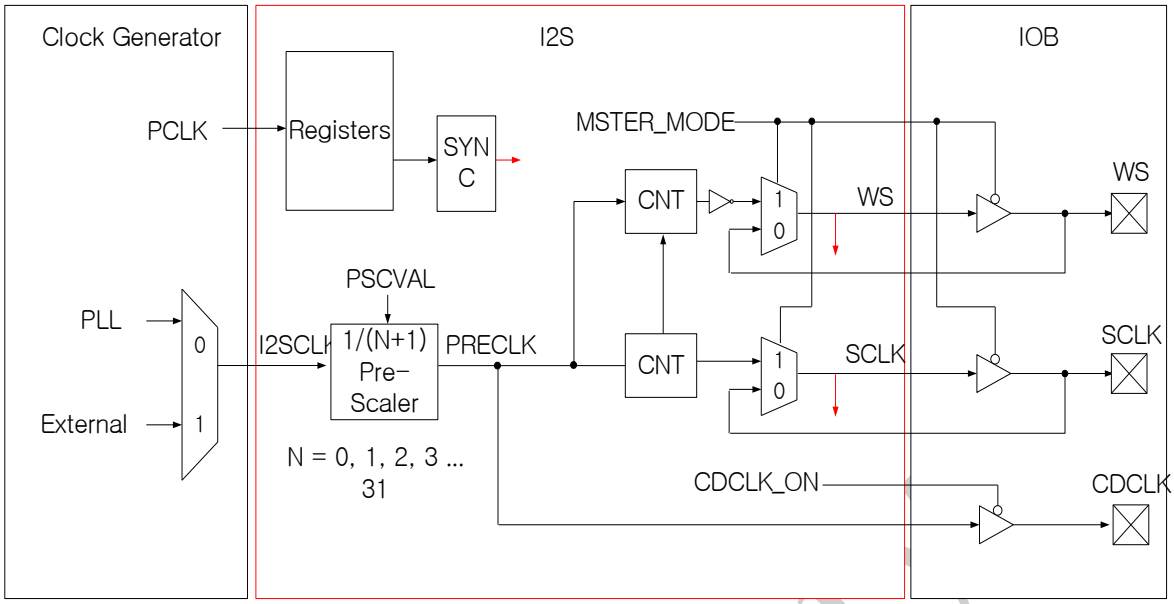
- I2S-bus, MSB-justified 2's complement format.
- Embedded Voice Codec interface.
- IMA-ADPCM Codec compatible
- 8/16-bit PCM data support.
- 16, 32, 48, 64 fs serial bit clock per channel. (fs : sampling frequency)
- 256, 384, 512 fs master clock.
- 128Bytes FIFOs for transmits and receives.

24.2 Block Description

24.2.1 Top block diagram

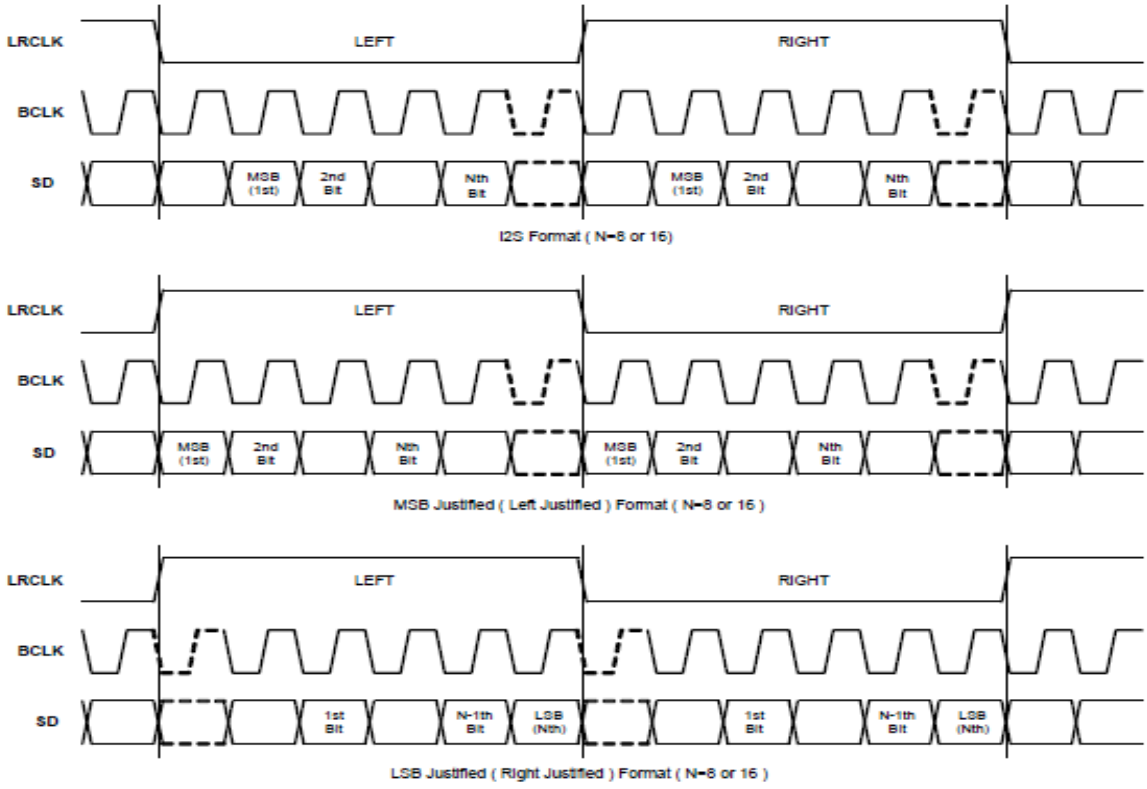


24.2.2 Clock Control block diagram



24.3 Function Description

24.3.1 TX RX Data Format



24.3.2 TX RX FIFO Format

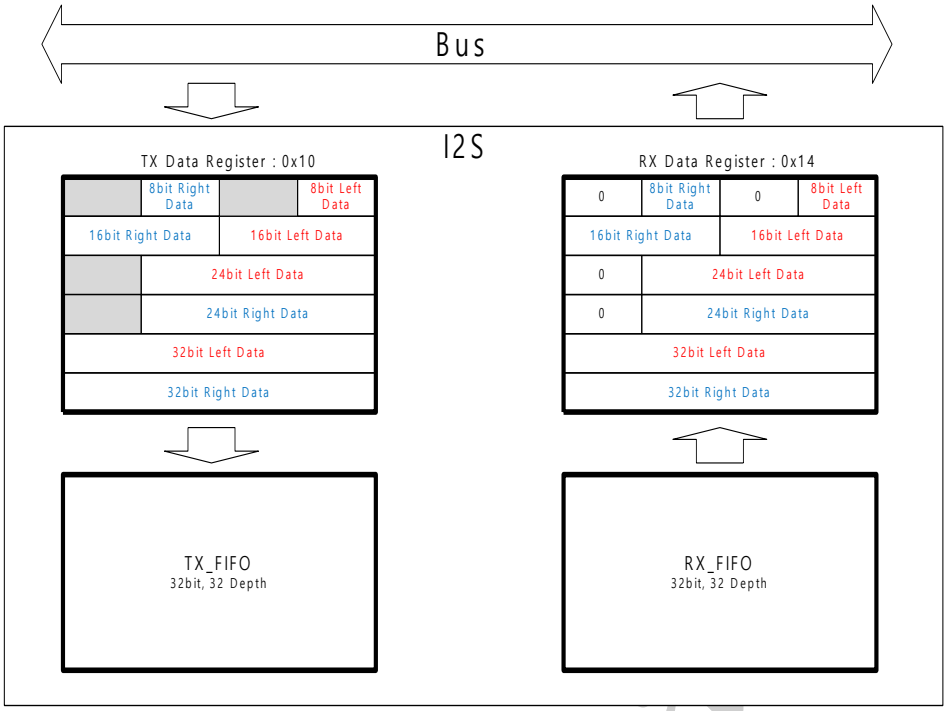
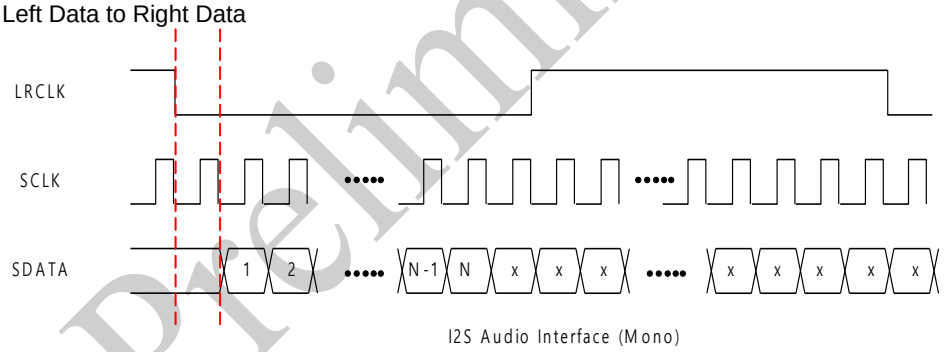


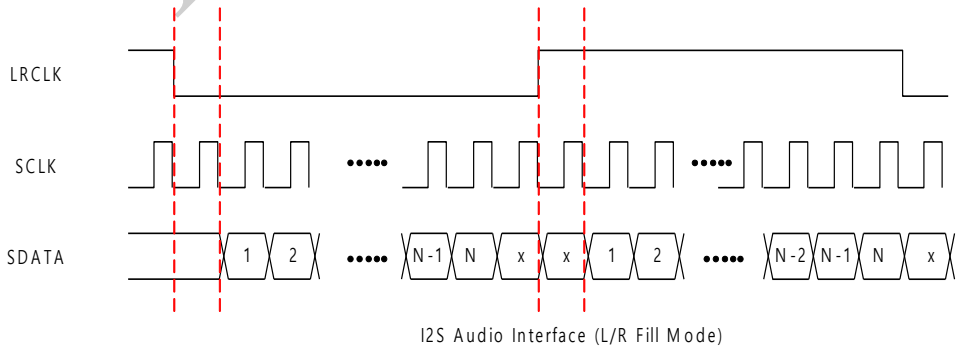
Figure 24-1 24bit, 32bit FIFO Data Format

24.3.3 Mono Data Extension

Copy to Left Data to Right Data



Before



After

Figure 24-2 Mono Data Extension

24.3.4 Clock Driving Master

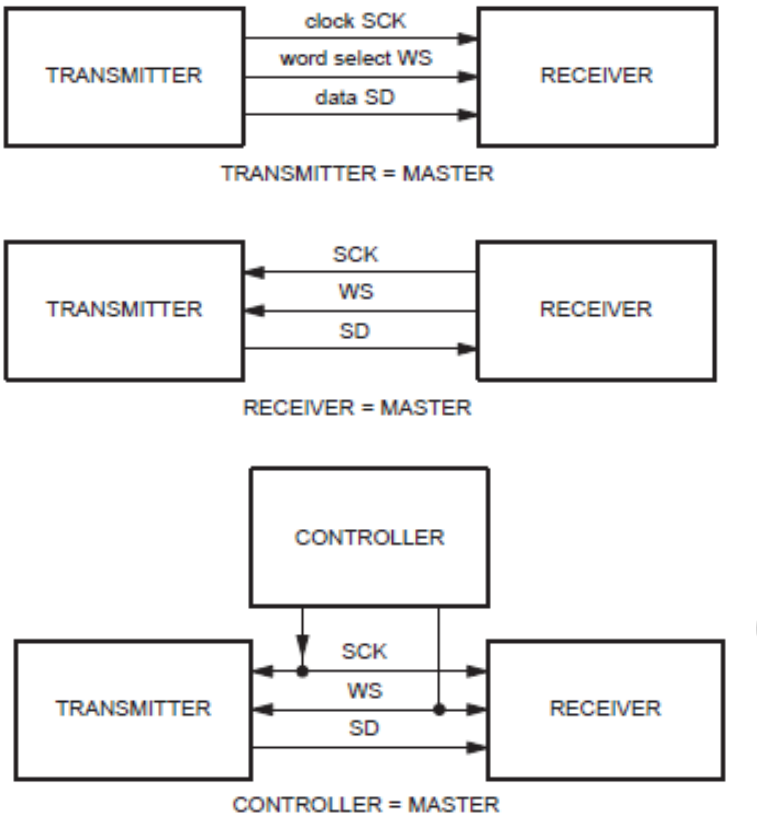


Figure 24-3 LRCLK and SCLK Master

24.3.5 Sampling Frequency

Table 36-1. CODEC clock (CODECLK = 256fs, 384fs, 512fs, 768fs)

IISLRCK (fs)	8.000 kHz	11.025 kHz	16.000 kHz	22.050 kHz	32.000 kHz	44.100 kHz	48.000 kHz	64.000 kHz	88.200 kHz	96.000 kHz
CODECLK (MHz)	256fs									
	2.0480	2.8224	4.0960	5.6448	8.1920	11.2896	12.2880	16.3840	22.5792	24.5760
	384fs									
	3.0720	4.2336	6.1440	8.4672	12.2880	16.9344	18.4320	24.5760	33.8688	36.8640
	512fs									
	4.0960	5.6448	8.1920	11.2900	16.3840	22.5790	24.5760	32.7680	45.1580	49.1520
	768fs									
	6.1440	8.4672	12.2880	16.9340	24.5760	33.8690	36.8640	49.1520	-	-

Note : fs represents sampling frequency.

CODECLK Frequency = fs * (256 or 384 or 512 or 768)

Figure 24-4 Sampling and Codec Clock Example

Clock Frequency		RFS			
		256 fs (00B)	512 fs (01B)	384 fs (10B)	768 fs (11B)
BFS	16 fs (10B)	(a)	(a)	(a)	(a)
	24 fs (11B)	-	-	(a)	(a)
	32 fs (00B)	(a) (b)	(a) (b)	(a) (b)	(a) (b)
	48 fs (01B)	-	-	(a) (b) (c)	(a) (b) (c)
Descriptions		(a) Allowed when BLC is 8-bit (b) Allowed when BLC is 16-bit (c) Allowed when BLC is 24-bit			

Note : Bit Clock Frequency ≥ fs * (bit length * 2). The codec clock is a multiple of the bit clock.

Figure 24-5 Support Sampling Codec Clock

24.4 Register Description

24.4.1 I2S Status Register (I2SFIC)

Address : 0xF400_4400 / 0xF400_4440

Bit	R/W	Description	Default value
31 : 22	R		
21 : 20	R	Left/Right channel clock indication. Note that LRI meaning depends on the value of LRP bit of I2SMOD register. 0 : Left(when LRP bit is low) or right (when LRP bit is high)	
19	R	Tx FIFO under-run interrupt status 0 : Interrupt does not occur 1 : Interrupt has been occurred	
18 : 12	R	Tx FIFO data count. FIFO has 16 depth. so value ranges from 0 to 16 N : Data count N of FIFO	
11	R	Tx FIFO empty status indication 0 : FIFO is not empty (ready to transmit) 1 : FIFO is empty (not ready to transmit)	
10	R	Tx FIFO Full status indication 0 : FIFO is not full 1 : FIFO is full	
9	R	Rx FIFO under-run interrupt status 0 : Interrupt does not occur 1 : Interrupt has been occurred	
8 : 2	R	Rx FIFO data count. FIFO has 16 depth. so value ranges from 0 to 16 N : Data count N of FIFO	
1	R	Rx FIFO empty status indication 0 : FIFO is not empty 1 : FIFO is empty	
0	R	Rx FIFO full status indication 0 : FIFO is not full (ready to receive data) 1 : FIFO is full (not ready to receive data)	

24.4.2 I2S Control Register (I2SCON)

Address : 0xF400_4404 / 0xF400_4444

Bit	R/W	Description	Default value
31 : 27	R	Reserved. Program to zero	0
26 : 20	R/W	Tx FIFO over-run threshold level (Range : 0 ~ 64)	0
19	R/W	Tx FIFO flush command 0 : No Operation 1 : Interrupt Clear	0
18	R/W	Tx FIFO under-run interrupt. you can do interrupt clear by writing '1' 0 : No Operation 1 : Interrupt Clear	0
17	R/W	Tx FIFO over-run interrupt Enable (Only for ch0) 0 : Tx FIFO over-run INT disable 1 : Tx FIFO over-run INT enable	0
16	R/W	Tx DMA operation pause command. Note that when this bit is activated at any time. the	

		DMA request will be halted after current on going DMA transfer is completed. 0 : No pause DMA operation 1 : Pause DMA operation	0
15	R/W	Tx DMA active (start DMA request). Note that when this bit is set form high to low, the DMA operation will be forced to stop immediately 0 : Inactive 1 : Active	0
14	R/W	Tx channel operation pause command. Note that when this bit is activated at any time the channel operation will be halted after left-right channel data transfer is completed 0 : No pause operation 1 : Pause operation	0
13 : 7	R/W	Rx FIFO over-run threshold level (Range : 0 ~ 64)	0
6	R/W	Rx FIFO flush command 0 : No Operation 1 : Interrupt Clear	0
5	R/W	Rx FIFO under-run interrupt. you can do interrupt clear by writing '1' 0 : No Operation 1 : Interrupt Clear	0
4	R/W	Rx FIFO over-run interrupt Enable (Only for ch0) 0 : Rx FIFO over-run INT disable 1 : Rx FIFO over-run INT enable	0
3	R/W	Rx DMA operation pause command. Note that when this bit is activated at any time. the DMA request will be halted after current on going DMA transfer is completed. 0 : No pause DMA operation 1 : Pause DMA operation	0
2	R/W	Rx DMA active (start DMA request). Note that when this bit is set form high to low, the DMA operation will be forced to stop immediately 0 : Inactive 1 : Active	0
1	R/W	Rx channel operation pause command note that when this bit is activated at any time. the channel operation will be halted after left-right channel data transfer is completed 0 : No pause operation 1 : Pause operation	0
0	R/W	I2S interface active (start operation) 0 : Inactive 1 : Active	0

24.4.3 I2S Mode Register (I2SMOD)

Address : 0xF400_4408 / 0xF400_4448

Bit	*R/W*	*Description*	*Default value*
31 : 18	R/W	Reserved.	0
17 : 16	R/W	Bit Length Control Bit Which decides transmission of 8/16 bits per audio channel 00: 16 Bits per channel 01: 24 Bits Per Channel 10: 32 Bits Per Channel 11: 8 Bits Per Channel	0
15	R/W	Codec clock On/Off 0 : codec clock Off 1 : codec clock On	0
14 : 13	R/W	I2S master (internal/external) or slave mode select. 00: Rx Tx Master mode 01: Rx Master Tx Slave mode 10: Rx Slave Tx Master mode 11: Rx Tx Slave mode	0
12 : 11	R/W	Transmit or receive mode select. 00: Transmit and receive simultaneous mode 01: Transmit only mode 10: Receive only mode 11: Reserved	0
10 : 9	R/W	Mono Data Extension 00: Transmit and receive extension mode 01: Transmit only extension mode 10: Receive only extension mode 11: Transmit and receive normal mode	0
8	R/W	Stereo/Mono Mode select. 0: Stereo 1: Mono	0
7	R/W	Bit clock polarity select. 0: Negative Active Serial Data 1: Positive Active Serial Data	0
6	R/W	Left/Right channel clock polarity select. 0 : Low for left channel and high for right channel 1 : High for left channel and low for right channel	0
5 : 4	R/W	Serial data format. 00 : I2S format 01 : MSB-justified (left-justified) format 10 : LSB-justified (right-justified) format	0

		11 : Reserved	
3 : 2	R/W	I2S root clock (codec clock) frequency select 00 : 256 fs 01 : 512 fs 10 : 384 fs 11 : 768 fs	0
1 : 0	R/W	Bit clock frequency select (if 32fs : channel per 32 psc_clock) 00 : 32 fs 01 : 48 fs 10 : 64 fs 11 : 16 fs	0

24.4.4 I2S Prescaler selection Register (I2SPSR)

Address : 0xF400_440C / 0xF400_444C

Bit	*R/W*	*Description*	*Default value*
31 : 9	R	Reserved	
8	R/W	Pre-scaler (clock divider) active. 0 : Inactive 1 : Active	
7 : 5	R	Reserved	
4 : 0	R/W	Pre-scaler (Clock divider) division value. N: Division factor is N+1 (N==0: bypass) After PSCREN=1, PSCVAL don't changing (recommend) 00000 : 1 00001 : 2 00010 : 3 00011 : 4 00100 : 5 00101 : 6 00110 : 7 00111 : 8 01000 : 9 01001 : 10 01010 : 11 01011 : 12 01100 : 13 01101 : 14 01110 : 15 01111 : 16 10000 : 17 10001 : 18 10010 : 19 10011 : 20 10100 : 21 10101 : 22 10110 : 23 10111 : 24 11000 : 25 11001 : 26 11010 : 27 11011 : 28 11100 : 29 11101 : 30 11110 : 31 11111 : 32	

24.4.5 I2S Tx Data FIFO (I2SPSR)

Address : 0xF400_4410 / 0xF400_4450

Bit	*R/W*	*Description*	*Default value*
31 : 0	W	TX FIFO write data. Note that the left/right channel data is allocated as the following bit fields. R[31:00], L[31:0] when 32-bit BLC R[23:00], L[23:0] when 24-bit BLC R[31:16], L[15:0] when 16-bit BLC R[23:15], L[07:0] when 8-bit BLC (Mono normal : L[07:0])	

24.4.6 I2S Rx Data FIFO (I2SPSR)

Address : 0xF400_4414 / 0xF400_4454

Bit	*R/W*	*Description*	*Default value*
31 : 0	R	RX FIFO read data. Note that the left/right channel data is allocated as the following bit fields. R[31:00], L[31:0] when 32-bit BLC R[23:00], L[23:0] when 24-bit BLC R[31:16], L[15:0] when 16-bit BLC R[23:15], L[07:0] when 8-bit BLC (Mono normal : L[07:0])	

25 GPIO (General Purpose I/O)

The GPIO Ports are composed of 8-bit 14 blocks and 4-bit 1 block. The GPIO provides totally 116 I/O ports.
Each port can be configured with register easily, and can be used for various input/output and system organization.

25.1 Features

- GP0.x has 8 I/O Ports
- GP1.x has 8 I/O Ports
- GP2.x has 8 I/O ports
- GP3.x has 8 I/O ports
- GP4.x has 8 I/O Ports
- GP5.x has 8 I/O Ports
- GP6.x has 8 I/O ports
- GP7.x has 8 I/O ports
- GP8.x has 8 I/O Ports
- GP9.x has 8 I/O Ports
- GP10.x has 8 I/O Ports
- GP11.x has 8 I/O Ports
- GP12.x has 4 I/O Ports
- GP13.x has 8 I/O Ports
- GP14.x has 8 I/O Ports

25.2 Block Diagram

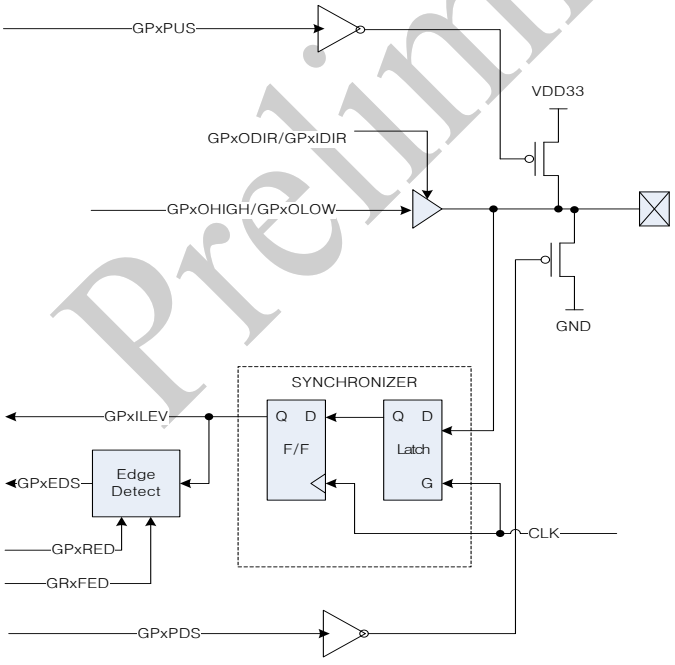


Figure 25-1 GPIO Block Diagram

25.3 Function Description

25.3.1 Port Control

GPIO Ports are configured as Output mode by GPxODIR register and configured as Input mode by GPxIDIR register port by port. The configured status of each port is stored into GPxDIR register. When user configures GPxODIR register and GPxIDIR register, the value of bit is 1 is configured, as the corresponding operation and that of bit is 0 does not affect anything.

The output level of GPIO Ports is set to High Level via GPxOHIGH register under Output mode and is set to Low Level via GPxOLOW register. The status of Output Level can be confirmed by checking GPxOLEV register.

The Input level of GPIO can be confirmed by checking GPxILEV. The Pull-up resistance is connected to each port. User can reduce leakage current if use removes Pull-up under the external input exists or ouput.

Table 25-1 Internal Pull-up Resistance Characteristics

Parameter	*Min*	*Typ*	*Max*	*Unit*
Pull-Up Resistance	34	41	64	KΩ
Pull-Down Resistance	33	44	79	KΩ

25.3.2 Port Edge Detect

External interrupt can be performed for each group by GPIO's Port Edge Detect as well as EIRQ pin. The port provides Rising Edge, Falling Edge and Any Edge modes.

25.4 Register Description

25.4.1 Port Direction Registers (GPxDIR)

Address: 0xF000_1C00 / 0xF000_1C40 / 0xF000_1C80 / 0xF000_1CC0
0xF000_1D00 / 0xF000_1D40 / 0xF000_1D80 / 0xF000_1DC0
0xF000_1E00 / 0xF000_1E40 / 0xF000_1E80 / 0xF000_1EC0
0xF000_1F00 / 0xF000_1F40 / 0xF000_1F80

Bit	*R/W*	*Description*	*Default value*
31 : 9	R	Reserved	-
8	R	GPx.OMD : GPx. Output Control Mode bit 0 : Pin 단위 1 : Port 단위	0
7 : 0	R	GPx.yDIR : GPx.y Direction bit 0 : Input 1 : Output	0x00

25.4.2 Port Direction Output Mode Setting Registers (GPxODIR)

Address: 0xF000_1C00 / 0xF000_1C40 / 0xF000_1C80 / 0xF000_1CC0
0xF000_1D00 / 0xF000_1D40 / 0xF000_1D80 / 0xF000_1DC0
0xF000_1E00 / 0xF000_1E40 / 0xF000_1E80 / 0xF000_1EC0
0xF000_1F00 / 0xF000_1F40 / 0xF000_1F80

Bit	*R/W*	*Description*	*Default value*
31 : 9	R	Reserved	-
8	W	GPx.OPRT : Output Control by Port Mode Setting bit	-
7	W	GPx.7ODIR : GPx.7 Direction Output Mode Setting bit	-
6	W	GPx.6ODIR : GPx.6 Direction Output Mode Setting bit	-
5	W	GPx.5ODIR : GPx.5 Direction Output Mode Setting bit	-
4	W	GPx.4ODIR : GPx.4 Direction Output Mode Setting bit	-
3	W	GPx.3ODIR : GPx.3 Direction Output Mode Setting bit	-
2	W	GPx.2ODIR : GPx.2 Direction Output Mode Setting bit	-
1	W	GPx.1ODIR : GPx.1 Direction Output Mode Setting bit	-
0	W	GPx.0ODIR : GPx.0 Direction Output Mode Setting bit	-

*** Port Direction Output Mode Setting bit
0 : No effect 1 : Set to output mode the corresponding bit in the PxDIR registers

25.4.3 Port Direction Input Mode Setting Registers (GPxIDIR)

Address: 0xF000_1C04 / 0xF000_1C44 / 0xF000_1C84 / 0xF000_1CC4
0xF000_1D04 / 0xF000_1D44 / 0xF000_1D84 / 0xF000_1DC4
0xF000_1E04 / 0xF000_1E44 / 0xF000_1E84 / 0xF000_1EC4
0xF000_1F04 / 0xF000_1F44 / 0xF000_1F84

Bit	R/W	Description	Default value
31 : 8	R	Reserved	-
8	W	GPx.OPIN : Output Control by Pin Mode Setting bit	-
7	W	GPx.7IDIR : GPx.7 Direction Input Mode Setting bit	-
6	W	GPx.6IDIR : GPx.6 Direction Input Mode Setting bit	-
5	W	GPx.5IDIR : GPx.5 Direction Input Mode Setting bit	-
4	W	GPx.4IDIR : GPx.4 Direction Input Mode Setting bit	-
3	W	GPx.3IDIR : GPx.3 Direction Input Mode Setting bit	-
2	W	GPx.2IDIR : GPx.2 Direction Input Mode Setting bit	-
1	W	GPx.1IDIR : GPx.1 Direction Input Mode Setting bit	-
0	W	GPx.0IDIR : GPx.0 Direction Input Mode Setting bit	-

*** Port Direction Input Mode Setting bit
0 : No effect 1 : Set to input mode the corresponding bit in the PxDIR registers

25.4.4 Port Output Data Level Registers (GPxOLEV)

Address: 0xF000_1C08 / 0xF000_1C48 / 0xF000_1C88 / 0xF000_1CC8
0xF000_1D08 / 0xF000_1D48 / 0xF000_1D88 / 0xF000_1DC8
0xF000_1E08 / 0xF000_1E48 / 0xF000_1E88 / 0xF000_1EC8
0xF000_1F08 / 0xF000_1F48 / 0xF000_1F88

Bit	R/W	Description	Default value
31 : 8	R	Reserved	-
7 : 0	R	GPx.yOLEV : GPx.y Output Level bit 0 : Low Level 1 : High Level	0xFF

25.4.5 Port Output Data Registers (GPxDOUT)

Address: 0xF000_1C08 / 0xF000_1C48 / 0xF000_1C88 / 0xF000_1CC8
0xF000_1D08 / 0xF000_1D48 / 0xF000_1D88 / 0xF000_1DC8
0xF000_1E08 / 0xF000_1E48 / 0xF000_1E88 / 0xF000_1EC08
0xF000_1F08 / 0xF000_1F48 / 0xF000_1F88

Bit	R/W	Description	Default value
7 : 0	R/W	GPx.DO : GPx.Port Output Data	0xFF

*** If the value of GPxDIR[8] is 1, It decides GPIO Port ouput by the register.

25.4.6 Port Output Data High Level Setting Registers (GPxOHIGH)

Address: 0xF000_1C08 / 0xF000_1C48 / 0xF000_1C88 / 0xF000_1CC8
0xF000_1D08 / 0xF000_1D48 / 0xF000_1D88 / 0xF000_1DC8
0xF000_1E08 / 0xF000_1E48 / 0xF000_1E88 / 0xF000_1EC8
0xF000_1F08 / 0xF000_1F48 / 0xF000_1F88

Bit	R/W	Description	Default value
31 : 8	R	Reserved	-
7	W	GPx.7OH : GPx.7 Output Data High Level Setting bit	-
6	W	GPx.6OH : GPx.6 Output Data High Level Setting bit	-
5	W	GPx.5OH : GPx.5 Output Data High Level Setting bit	-
4	W	GPx.4OH : GPx.4 Output Data High Level Setting bit	-
3	W	GPx.3OH : GPx.3 Output Data High Level Setting bit	-
2	W	GPx.2OH : GPx.2 Output Data High Level Setting bit	-
1	W	GPx.1OH : GPx.1 Output Data High Level Setting bit	-
0	W	GPx.0OH : GPx.0 Output Data High Level Setting bit	-

*** Port Output Data High Level Setting bit (available when GPxDIR[8]is 0.)
0 : No effect
1 : Set to high level output data the corresponding bit in the PxOLEV registers

25.4.7 Port Output Data Low Level Setting Registers (GPxOLOW)

Address: 0xF000_1C0C / 0xF000_1C4C / 0xF000_1C8C / 0xF000_1CCC
0xF000_1D0C / 0xF000_1D4C / 0xF000_1D8C / 0xF000_1DCC
0xF000_1E0C / 0xF000_1E4C / 0xF000_1E8C / 0xF000_1ECC
0xF000_1F0C / 0xF000_1F4C / 0xF000_1F8C

Bit	R/W	Description	Default value
31 : 8	R	Reserved	-
7	W	GPx.7OL : GPx.7 Output Data Low Level Setting bit	-
6	W	GPx.6OL : GPx.6 Output Data Low Level Setting bit	-
5	W	GPx.5OL : GPx.5 Output Data Low Level Setting bit	-
4	W	GPx.4OL : GPx.4 Output Data Low Level Setting bit	-
3	W	GPx.3OL : GPx.3 Output Data Low Level Setting bit	-
2	W	GPx.2OL : GPx.2 Output Data Low Level Setting bit	-
1	W	GPx.1OL : GPx.1 Output Data Low Level Setting bit	-
0	W	GPx.0OL : GPx.0 Output Data Low Level Setting bit	-

*** Port Output Data Low Level Setting bit (available when GPxDIR[8]is 0.)
0 : No effect
1 : Set to low level output data the corresponding bit in the PxOLEV registers

25.4.8 Port Input Data Level Registers (GPxILEV)

Address: 0xF000_1C10 / 0xF000_1C50 / 0xF000_1C90 / 0xF000_1CD0
0xF000_1D10 / 0xF000_1D50 / 0xF000_1D90 / 0xF000_1DD0
0xF000_1E10 / 0xF000_1E50 / 0xF000_1E90 / 0xF000_1ED0
0xF000_1F10 / 0xF000_1F50 / 0xF000_1F90

Bit	R/W	Description	Default value
31 : 8	R	Reserved	-
7	R	GPx.7ILEV : GPx.7 Input Level bit 0 : Low Level 1 : High Level	-
6	R	GPx.6ILEV : GPx.6 Input Level bit 0 : Low Level 1 : High Level	-
5	R	GPx.5ILEV : GPx.5 Input Level bit 0 : Low Level 1 : High Level	-
4	R	GPx.4ILEV : GPx.4 Input Level bit 0 : Low Level 1 : High Level	-
3	R	GPx.3ILEV : GPx.3 Input Level bit 0 : Low Level 1 : High Level	-
2	R	GPx.2ILEV : GPx.2 Input Level bit 0 : Low Level 1 : High Level	-
1	R	GPx.1ILEV : GPx.1 Input Level bit 0 : Low Level 1 : High Level	-
0	R	GPx.0ILEV : GPx.0 Input Level bit 0 : Low Level 1 : High Level	-

25.4.9 Port Pull-up Status Registers (GPxPUS)

Address: 0xF000_1C18 / 0xF000_1C58 / 0xF000_1C98 / 0xF000_1CD8
0xF000_1D18 / 0xF000_1D58 / 0xF000_1D98 / 0xF000_1DD8
0xF000_1E18 / 0xF000_1E58 / 0xF000_1E98 / 0xF000_1ED8
0xF000_1F18 / 0xF000_1F58 / 0xF000_1F98

Bit	R/W	Description	Default value
31 : 8	R	Reserved	-
7 : 0	R	GPx.yUP : GPx.y Pull-up Status bit 0 : Pull-up Disable 1 : Pull-up Enable	0xffn

25.4.10 Port Pull-up Enable Registers (GPxPUEN)

Address: 0xF000_1C18 / 0xF000_1C58 / 0xF000_1C98 / 0xF000_1CD8
0xF000_1D18 / 0xF000_1D58 / 0xF000_1D98 / 0xF000_1DD8
0xF000_1E18 / 0xF000_1E58 / 0xF000_1E98 / 0xF000_1ED8
0xF000_1F18 / 0xF000_1F58 / 0xF000_1F98

Bit	R/W	Description	Default value
31 : 8	R	Reserved	-
7	W	GPx.7PUEN : GPx.7 Pull-up enable bit	-
6	W	GPx.6PUEN : GPx.6 Pull-up enable bit	-
5	W	GPx.5PUEN : GPx.5 Pull-up enable bit	-
4	W	GPx.4PUEN : GPx.4 Pull-up enable bit	-
3	W	GPx.3PUEN : GPx.3 Pull-up enable bit	-
2	W	GPx.2PUEN : GPx.2 Pull-up enable bit	-
1	W	GPx.1PUEN : GPx.1 Pull-up enable bit	-
0	W	GPx.0PUEN : GPx.0 Pull-up enable bit	-

*** Port Pull-up enable bit
0 : No effect
1 : Set to pull-up the corresponding bit in the PxPUS registers

25.4.11 Port Pull-up Disable Registers (GPxPUDIS)

Address: 0xF000_1C1C / 0xF000_1C5C / 0xF000_1C9C / 0xF000_1CDC
0xF000_1D1C / 0xF000_1D5C / 0xF000_1D9C / 0xF000_1DDC
0xF000_1E1C / 0xF000_1E5C / 0xF000_1E9C / 0xF000_1EDC
0xF000_1F1C / 0xF000_1F5C / 0xF000_1F9C

Bit	R/W	Description	Default value
31 : 8	R	Reserved	-
7	W	GPx.7PUDIS : GPx.7 Pull-up disable bit	-
6	W	GPx.6PUDIS : GPx.6 Pull-up disable bit	-
5	W	GPx.5PUDIS : GPx.5 Pull-up disable bit	-
4	W	GPx.4PUDIS : GPx.4 Pull-up disable bit	-
3	W	GPx.3PUDIS : GPx.3 Pull-up disable bit	-
2	W	GPx.2PUDIS : GPx.2 Pull-up disable bit	-
1	W	GPx.1PUDIS : GPx.1 Pull-up disable bit	-
0	W	GPx.0PUDIS : GPx.0 Pull-up disable bit	-

*** Port Pull-up disable bit
0 : No effect
1 : Set to pull-up the corresponding bit in the PxPUS registers

25.4.12 Port Rising Edge Detect Registers (GPxRED)

Address: 0xF000_1C20 / 0xF000_1C60 / 0xF000_1CA0 / 0xF000_1CE0
0xF000_1D20 / 0xF000_1D60 / 0xF000_1DA0 / 0xF000_1DE0
0xF000_1E20 / 0xF000_1E60 / 0xF000_1EA0 / 0xF000_1EE0
0xF000_1F20 / 0xF000_1F60 / 0xF000_1FA0

Bit	R/W	Description	Default value
31 : 8	R	Reserved	-
7	R/W	GPx.7RED : GPx.7 Rising Edge Detect bit 0 : Disable 1 : Enable	0
6	R/W	GPx.6RED : GPx.6 Rising Edge Detect bit 0 : Disable 1 : Enable	0
5	R/W	GPx.5RED : GPx.5 Rising Edge Detect bit 0 : Disable 1 : Enable	0
4	R/W	GPx.4RED : GPx.4 Rising Edge Detect bit 0 : Disable 1 : Enable	0
3	R/W	GPx.3RED : GPx.3 Rising Edge Detect bit 0 : Disable 1 : Enable	0
2	R/W	GPx.2RED : GPx.2 Rising Edge Detect bit 0 : Disable 1 : Enable	0
1	R/W	GPx.1RED : GPx.1 Rising Edge Detect bit 0 : Disable 1 : Enable	0
0	R/W	GPx.0RED : GPx.0 Rising Edge Detect bit 0 : Disable 1 : Enable	0

*** When both Rising Edge and Falling Edge are set, Edge detect mode becomes Any Edge mode.

25.4.13 Port Falling Edge Detect Registers (GPxFED)

Address: 0xF000_1C24 / 0xF000_1C64 / 0xF000_1CA4 / 0xF000_1CE4
0xF000_1D24 / 0xF000_1D64 / 0xF000_1DA4 / 0xF000_1DE4
0xF000_1E24 / 0xF000_1E64 / 0xF000_1EA4 / 0xF000_1EE4
0xF000_1F24 / 0xF000_1F64 / 0xF000_1FA4

Bit	*R/W*	*Description*	*Default value*
31 : 8	R	Reserved	-
7	R/W	GPx.7FED : GPx.7 Falling Edge Detect bit 0 : Disable 1 : Enable	0
6	R/W	GPx.6FED : GPx.6 Falling Edge Detect bit 0 : Disable 1 : Enable	0
5	R/W	GPx.5FED : GPx.5 Falling Edge Detect bit 0 : Disable 1 : Enable	0
4	R/W	GPx.4FED : GPx.4 Falling Edge Detect bit 0 : Disable 1 : Enable	0
3	R/W	GPx.3FED : GPx.3 Falling Edge Detect bit 0 : Disable 1 : Enable	0
2	R/W	GPx.2FED : GPx.2 Falling Edge Detect bit 0 : Disable 1 : Enable	0
1	R/W	GPx.1FED : GPx.1 Falling Edge Detect bit 0 : Disable 1 : Enable	0
0	R/W	GPx.0FED : GPx.0 Falling Edge Detect bit 0 : Disable 1 : Enable	0

*** When both Rising Edge and Falling Edge are set, Edge detect mode becomes Any Edge mode.

25.4.14 Port Edge Detect Status Registers (GPxEDS)

Address: 0xF000_1C28 / 0xF000_1C68 / 0xF000_1CA8 / 0xF000_1CE8
0xF000_1D28 / 0xF000_1D68 / 0xF000_1DA8 / 0xF000_1DE8
0xF000_1E28 / 0xF000_1E68 / 0xF000_1EA8 / 0xF000_1EE8
0xF000_1F28 / 0xF000_1F68 / 0xF000_1FA8

Bit	*R/W*	*Description*	*Default value*
31 : 8	R	Reserved	-
7	R/W	GPx.7EDS : GPx.7 Edge Detect Status bit	0
6	R/W	GPx.6EDS : GPx.6 Edge Detect Status bit	0
5	R/W	GPx.5EDS : GPx.5 Edge Detect Status bit	0
4	R/W	GPx.4EDS : GPx.4 Edge Detect Status bit	0
3	R/W	GPx.3EDS : GPx.3 Edge Detect Status bit	0
2	R/W	GPx.2EDS : GPx.2 Edge Detect Status bit	0
1	R/W	GPx.1EDS : GPx.1 Edge Detect Status bit	0
0	R/W	GPx.0EDS : GPx.0 Edge Detect Status bit	0

*** Port Edge Detect Status bit
0 : No edge detect has occurred on pin
1 : Edge detect has occurred on pin

*** Status bits are cleared by writing a one to them.
*** Writing a zero to a status bit are no effect.

25.4.15 Port Open Drain Mode Control Registers (GPxODM)

Address: 0xF000_1C2C / 0xF000_1C6C / 0xF000_1CAC / 0xF000_1CEC
0xF000_1D2C / 0xF000_1D6C / 0xF000_1DAC / 0xF000_1DEC
0xF000_1E2C / 0xF000_1E6C / 0xF000_1EAC / 0xF000_1EEC
0xF000_1F2C / 0xF000_1F6C / 0xF000_1FAC

Bit	*R/W*	*Description*	*Default value*
31 : 8	R	Reserved	-
7 : 0	R/W	GPx.yOD : GPx.y Open Drain Mode Setting bit 0 : Normal CMOS Output Mode 1 : Open Drain Mode	0

26 UART

The AMAZON-II has 5 channel UART(Universal Asynchronous Receiver/Transmitter) controller, and it allows asynchronous communication with general PC or I/O devices equipping RS-232 interface.

26.1 Features

- Compatible with standard 16450/16550 UARTs
- Fully programmable serial-interface protocols
  - 5,6,7,8-bit characters
  - Even, odd or no-parity, stick parity generation and detection
  - 1, 1.5, 2 stop bit generation
  - Baud rate generator
- Line break generation and detection
- False start bit detection
- Prioritized transmit, receive and line status control interrupts
- Independent 16 characters transmit and receive 16Bytes FIFOs
- 5 Ch. UARTs

26.2 Block Diagram

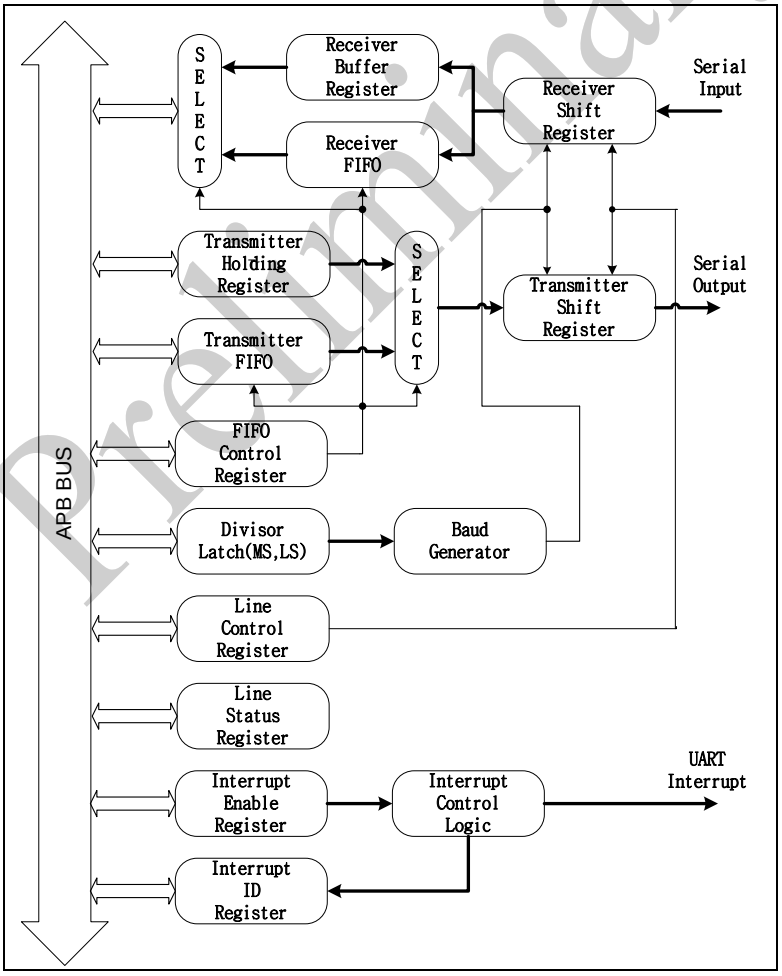
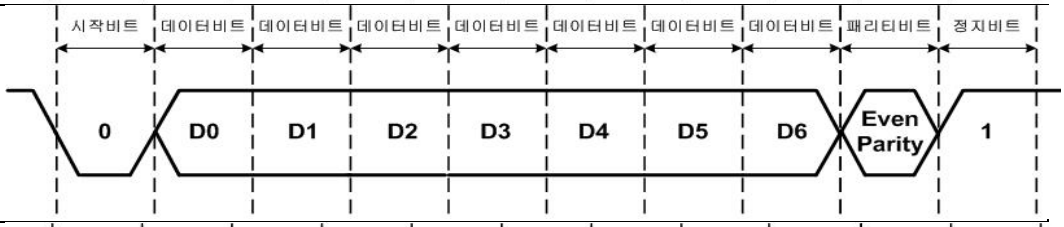


Figure 26-1 UART Block Diagram

26.3 Function Description

26.3.1 Serial Data Format

UART of the Amzon2 can change the serial data format of UART communication by configuring ULCRn[4:0] bits. Following table explains available data formats.

ULCRn[4:0]	*Description*
00010 No Parity / 1 Stop bit / 7 Data bit	
00011 No Parity / 1 Stop bit / 8 Data bit	
00110 No Parity / 2 Stop bit / 7 Data bit	
00111 No Parity / 2 Stop bit / 8 Data bit	
11010 Even Parity / 1 Stop bit / 7 Data bit	
11011 Even Parity / 1 Stop bit / 8 Data bit	

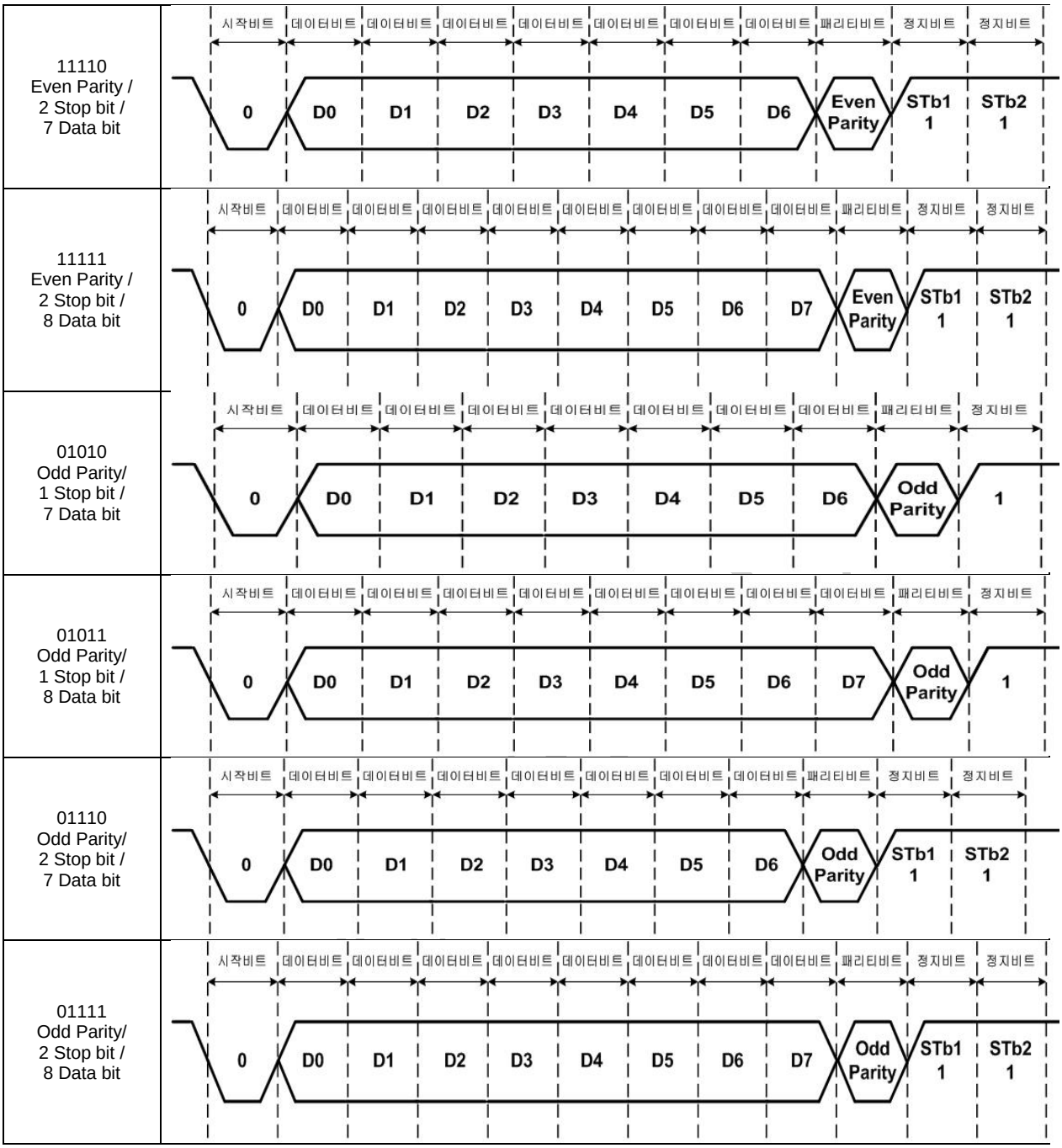


Figure 26-2 UART LCR Register Setting and Serial Data Format

26.3.2 UART Baud Rate

TX/RX Baud Rate can be calculated from the following equation.

$$UART\ \ Baud\ \ Rate = \frac{f_{PCLK}}{16\ \times\ UDL}$$

UART Divisor Latch Value (UDL) = UDLM[7:0] << 8 + UDLL[7:0]

Table 26-1 UART Baud Rate

f_{PCLK} (MHz)		1.024	2.048	5.6448	11.2896	24.0	48.0
2400 bps	UDL	27	53	147	294	625	1250
	ERR(%)	1.23	0.63	0.00	0.00	0.00	0.00
4800 bps	UDL	-	27	74	147	313	625
	ERR(%)	-	1.23	0.68	0.00	0.16	0.00
9600 bps	UDL	-	-	37	74	156	313
	ERR(%)	-	-	0.68	0.68	0.16	0.16
14400 bps	UDL	-	9	25	49	104	208
	ERR(%)	-	1.23	2.00	0.00	0.16	0.16
19200 bps	UDL	-	-	18	37	78	156
	ERR(%)	-	-	2.08	0.68	0.16	0.16
38400 bps	UDL	-	-	9	18	39	78
	ERR(%)	-	-	2.08	2.08	0.16	0.16
57600 bps	UDL	-	-	6	12	26	52
	ERR(%)	-	-	2.08	2.08	0.16	0.16
115200bps	UDL	-	-	3	6	13	26
	ERR(%)	-	-	2.08	2.08	0.16	0.16

*** UART is assumed to be unreliable when ERR is higher than 2.2

26.4 Register Summery

Table 26-2 UART Register Summery

Bit No.	DLAB = 0 0x00	DLAB = 0 0x00	DLAB = 0 0x04	DLAB = 0 0x08	DLAB = X 0x08	DLAB = X 0x0C	DLAB = X 0x14	DLAB = 1 0x00	DLAB = 1 0x04
	Receiver Buffer Register	Transmitter Holding Register	Interrupt Enable Register	Interrupt Ident. Register	FIFO Control Register	Line Control Register	Line Status Register	Divisor Latch (LSB)	Divisor Latch (MSB)
	RBR	THR	IER	IIR	FCR	LCR	LSR	DLL	DLM
	R	R/W	R/W	R	R/W	R/W	R	R/W	R/W
0	Data Bit 0	Data Bit 0	Enable Received Data Available Interrupt	"0" if Interrupt Pending	FIFO Enable	Word Length Select Bit 0	Data Ready	Bit 0	Bit 0
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt	Interrupt ID Bit 0	RCVR FIFO Reset	Word Length Select Bit 1	Overrun Error	Bit 1	Bit 1
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt	Interrupt ID Bit 1	XMIT FIFO Reset	Number of Stop Bits	Parity Error	Bit 2	Bit 2
3	Data Bit 3	Data Bit 3	0	Interrupt ID Bit 2	0	Parity Enable	Framing Error	Bit 3	Bit 3
4	Data Bit 4	Data Bit 4	0	0	Reserved	Even Parity Select	Break Interrupt	Bit 4	Bit 4
5	Data Bit 5	Data Bit 5	0	0	Reserved	Stick Parity	Transmitter Holding Register	Bit 5	Bit 5
6	Data Bit 6	Data Bit 6	0	FIFOs Enabled	RCVR Trigger(LSB)	Set Break	Transmitter Empty	Bit 6	Bit 6
7	Data Bit 7	Data Bit 7	0	FIFOs Enabled	RCVR Trigger(MSB)	Divisor Latch Access Bit (DLAB)	Error in RCVR FIFO	Bit 7	Bit 7

* DLAB = LCR[7](Divisor Latch Access Bit)
* FIFO Control Register :
  - DLAB = 0 : Register Write
  - DLAB = 1 : Register Read
* Address 0x10(0x30), 0x18(0x38), 0x1C(0x3C) is reserved to comply with 16550 UART

26.5 Register Description

26.5.1 UART Channel Receiver Buffer Registers (UxRB)

Address : 0xF400_3000 / 0xF400_3020 / 0xF400_3040 / 0xF400_3060

Bit	R/W	Description	Default value
31: 8	R	Reserved.	-
7 : 0	R	Receive Buffer Data	-

*** Accessible when DLAB is “0”.

26.5.2 UART Channel Transmitter Holding Registers (UxTH)

Address : 0xF400_3000 / 0xF400_3020 / 0xF400_3040 / 0xF400_3060

Bit	R/W	Description	Default value
31: 8	W	Reserved.	-
7 : 0	W	Transmit Holding Data	-

*** Accessible when DLAB is “0”.

26.5.3 UART Channel Interrupt Enable Registers (UxIE)

Address : 0xF400_3004 / 0xF400_3024 / 0xF400_3044 / 0xF400_3064

Bit	R/W	Description	Default value
31: 3	R	Reserved.	-
2	RW	RLSIEN : Receiver Line Status Interrupt Enable bit 0 : Disable 1 : Enable	0
1	RW	THEIEN : Transmitter Holding Empty Interrupt Enable bit 0 : Disable 1 : Enable	0
0	RW	RDAIEN : Received Data Available Interrupt Enable bit 0 : Disable 1 : Enable	0

*** Accessible when DLAB is “0”.

26.5.4 UART Channel Interrupt Identification Register (UxII)

Address : 0xF400_3008 / 0xF400_3028 / 0xF400_3048 / 0xF400_3068

Bit	R/W	Description	Default value
31 : 8	R	Reserved.	-
7 : 6	R	FIFOST : FIFOs Enabled Status bit. 00 : not in FIFO mode 11 : FIFO mode	00
5 : 4	R	Reserved	0
3 : 0	R	INTID : UART Interrupt ID (Note, UART Interrupt Control Function)	0001

*** Accessible in read mode only when DLAB is “0”.

Table 26-3 UART Interrupt Control Function

Interrupt Identification Register				Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Condition
Bit 3	Bit 2	Bit 1	Bit 0				
0	0	0	1	-	None	None	-
0	1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available or Trigger Level Reached	Reading the Receiver Buffer Register or the FIFO Drops Below the Trigger Level
1	1	0	0	Second	Character Timeout Indication	No Characters have been removed from or input to the RCVR FIFO during the last 4 Char. times, and there is at least 1 Char. in it during this Time	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register

26.5.5 UART Channel FIFO Control Register (UxFC)

Address : 0xF400_3008 / 0xF400_3028 / 0xF400_3048 / 0xF400_3068

Bit	R/W	Description	Default value
31 : 8	R	Reserved.	-
7 : 6	RW	RFTL : Receiver FIFO Trigger Level 00 : 1 Byte 01 : 4 Byte 10: 8 Byte 11 : 14 Byte	00
5 : 3	R	Reserved	-
2	RW	XFR : XMIT FIFO Reset All data in XMIT FIFO is reset when XFR is “1”. However, data is shift register isn’t reset.	0
1	RW	RFR : RCVR FIFO Reset All data in RCVR FIFO is reset when RFR is “1”. However, data is shift register isn’t reset.	0
0	RW	FIFOEN : FIFO Enable Bit 0 : 16450 UART Mode1 : Enables FIFO	0

*** DLAB = “0” ➔ write mode, DLAB =”1” ➔ read mode.

26.5.6 UART Channel Line Control Register (UxLC)

Address : 0xF400_300C / 0xF400_302C / 0xF400_304C / 0xF400_306C

Bit	R/W	Description	Default value
31 : 8	R	Reserved.	-
7	RW	DLAB : Divisor Latch Access Bit When this bit is “1”, divisor latch register can be read/written and FIFO control register can be read.	0
6	RW	SB : Set Break When this bit is “1”, serial data output pin outputs logic “0”. SB doesn’t affect internal transmitter logic. It only affects serial output.	0
5	RW	SP : Stick Parity 0 : Disables Stick Parity 1 : PEN, EPS, and SP are “1” ➔ Parity bit=”0” PEN and SP are “1”, EPS is “0” ➔ Parity bit=”1”	0
4	RW	EPS : Even Parity Select 0 : Select Odd Parity 1 : Select Even Parity	0
3	RW	PEN : Parity Enable Bit 0 : Disables Parity 1 : Enables Parity	0
2	RW	STB : Number of Stop Bit 0 : 1 Stop bit 1 : 2 Stop bits (If WLS bit is set to 00(=5bits/character), it will be 1.5 instead of 2	0
1 : 0	RW	WLS : Word Length Select 00 : 5 Bits/Character 01 : 6 Bits/Character 10 : 7 Bits/Character 11 : 8 Bits/Character	00

26.5.7 UART Channel Line Status Register (UxLS)

Address : 0xF400_3014 / 0xF400_3034 / 0xF400_3054 / 0xF400_3074

Bit	R/W	Description	Default value
31 : 8	R	Reserved.	-
7	R	EIRF : Error in RCVR FIFO If not in FIFO mode, EIRF is always “0”. In FIFO mode, EIRF become “1” if any of OE, PE, FE, or BI of RCVR FIFO is set “1”. EIRF is cleared (=”0”) when LSR register is read and FIFO doesn’t have consecutive errors.	0
6	R	TEMP : Transmitter Empty If not in FIFO mode, TEMT become “1” when both transmitter holding register (THR) and Transmitter shift register (TSR) are empty. If either of THR or TSR has data, it is cleared. In FIFO mode, it is set when both of transmitter FIFO and TSR are empty.	1
5	R	THRE : Transmitter Holding Register Empty If not in FIFO mode, THRE is set when THR become empty by transmitting data to TSR. At this moment, THR can be written new data to transmit. In FIFO mode, THRE is set when transmit FIFO is empty, and cleared when any byte is written into transmit FIFO. If both THRE interrupt (ETHREI) and THRE are “1”, interrupt raises.	1
4	R	BINT : Break Interrupt : BI is set when input data is “0” during the full word transmission time. Full word transmission time is the sum of start, data, parity, and stop bit transmission time. In FIFO mode, this error applies to each byte inside FIFO, and FIFO are cleared when BI happens. This bit is cleared when CPU reads LSR.	0
3	R	FERR : Framing Error FE is set when input data doesn’t have valid stop bit. In FIFO mode, this error applies to each byte inside FIFO. It is cleared when CPU reads LSR.	0
2	R	PERR : Parity Error PE is set when input data doesn’t coincide with parity bit chosen by LCR register. In FIFO mode, this error applies to each byte inside FIFO. It is cleared when CPU read LSR.	0
1	R	OERR : Overrun Error In not FIFO mode, OE is set when new data is written before data inside RBR is read. In FIFO mode, it is set if a new full word comes to receiver shift register (RSR) when FIFO is full. In this case, RSR is updated; however, FIFO doesn’t transmit. It is cleared when CPU reads LSR.	0
0	R	DRDY : Data Ready DR is set when received data is written on RBR or FIFO. It is cleared when every data inside RBR or FIFO is read.	0

26.5.8 UART Channel Divisor Latch LSB Register (UxDLL)

Address : 0xF400_3000 / 0xF400_3020 / 0xF400_3040 / 0xF400_3060

Bit	R/W	Description	Default value
31: 8	R	Reserved.	-
7 : 0	RW	Divisor Latch Least Significant Byte	0x00

*** Accessible when DLAB is “1”.

26.5.9 UART Channel Divisor Latch MSB Register (UxDLM)

Address : 0xF400_3004 / 0xF400_3024 / 0xF400_3044 / 0xF400_3064

Bit	R/W	Description	Default value
31: 8	R	Reserved.	-
7 : 0	RW	Divisor Latch Most Significant Byte	0x00

*** Accessible when DLAB is “1”.

26.5.10 UART IrDA Mode Register (UxIRM)

Address : 0xF400_3068

Bit	R/W	Description	Default value
31: 6	R	Reserved.	-
5	RW	IrDA Rx Polarity Inversion	0
4	RW	IrDA Rx Decoding Enable 0 : Not decoding 1 : decoding the IR Frame	0
3 : 2	R	Reserved	00
1	RW	IrDA Tx Polarity Inversion	0
0	RW	IrDA Tx Encoding Enable 0 : not encoding 1 : encoding the UART frame	0

27 Watchdog Timer

Watchdog Timer is responsible for rollback the system when CPU operates wrong execution due to system errors, device's wrong response, and noise.

If the watchdog time is enabled, the counter value WDTCNT is decreased by 1, and when the value becomes 0, Watchdog Reset is occurred.

If the Watchdog Reset is signaled, the status of the system is stored into WDTST bit.

In order to prevent Watchdog Reset from system under Watchdog Timer enabled, because 32-bit Watchdog Counter value should not be 0, developer should re-configure the WDTCNT.

If WDTMOD bit is set as Interrupt mode, system occurs Interrupt rather Watchdog Reset. In that case, the system informs that WDTCNT value is 0.

27.1 Register Description

27.1.1 Watchdog Timer Control Register (WDTCTRL)

Address : 0xF400_3400

Bit	*R/W*	*Description*	*Default value*
31 : 5	R	Reserved	-
4	R	WDTST : Watchdog timer status bit When watchdog timer is reset mode, 0 : No watchdog reset 1 : Watchdog reset When watchdog timer is interrupt mode, 0 : No watchdog interrupt 1 : Watchdog interrupt Clear at read	0
3 : 2	R	Reserved	-
1	R/W	WDTMOD : Watchdog timer mode select bit 0 : Reset mode 1 : Interrupt mode	0
0	R/W	WDTEN : Watchdog timer enable bit 0 : Disable 1 : Enable	0

27.1.2 Watchdog Timer Counter Value Register (WDTCNT)

Address : 0xF400_3404

Bit	*R/W*	*Description*	*Default value*
31 : 0	R/W	Watchdog timer counter 32-bit value. Down-counter	0xFFFFFFFF

28 Timers

The AMAZON-II includes 4-channel 16-bit timer/counter which support timer/counter, capture, and PWM functions.

28.1 Features

- 15-bit Pre-scale
- 32-bit Timer/Counter
- 32-bit Capture
- 32-bit PWM
- 32-bit Timer Counter Wave-Out

28.2 Function Description

28.2.1 15-bit Pre-scaler with clock source selection

Pre-scaler choose an input source between system clock and external clock with CLKSEL bit. It divides the input source by between 2 and 32768, and transfers the divided clock to timer/counter. Timer/counter receives the divided clock, and runs 32bit counter.

When precise phase of the divided clock is needed, pre-scaler counter should be initilaized by setting CNTCLR bit of TPxCPM register.

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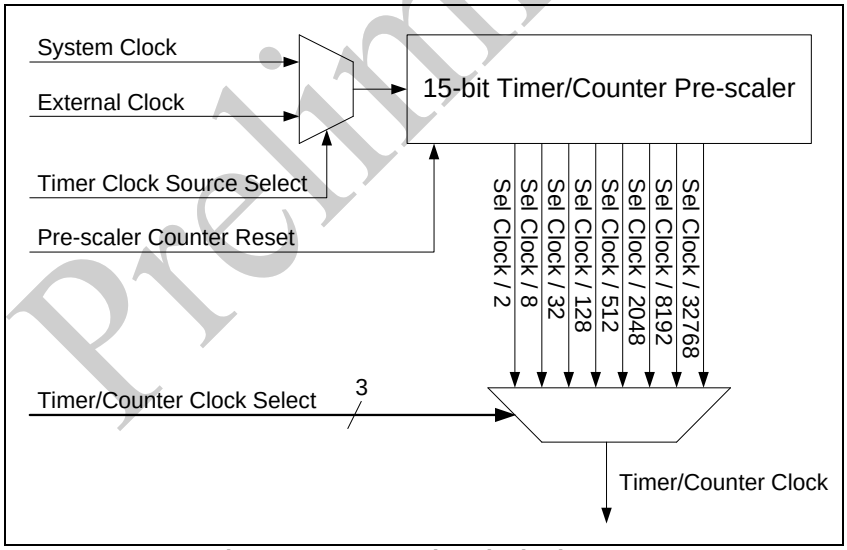


Figure 28-1 Pre-scaler Block Diagram

28.2.2 Timer/Counter

On every cycle of divided clock from pre-scaler, counter value is increment by one from 0x0 until it reaches the user-difined timer counter register value. When reached, the counter value is reset(=0) and interrupt raises.

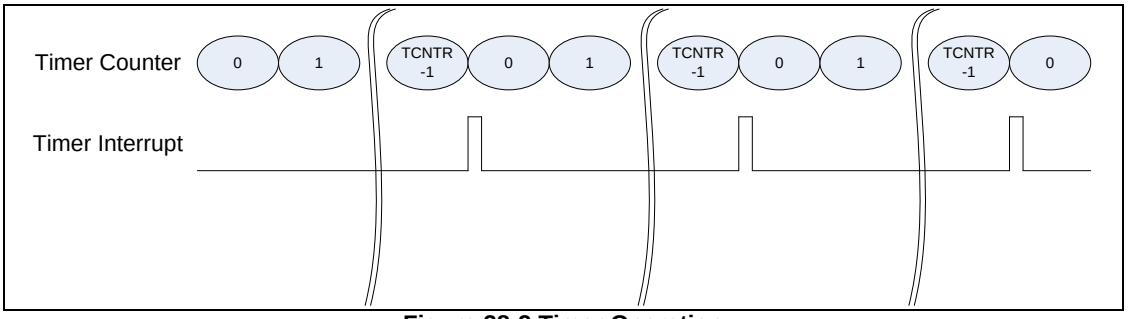


Figure 28-2 Timer Operation

The period of a timer is decided by selected clock, pre-scaler, and timer counter.

$$Timer\ \ Period = \frac{1}{Clock\ \ Source\ \ Frequency} \times \frac{1}{\Pr e - scaler\ \ Factor} \times (TMCNT)\ [\sec] \qquad \{\Pr e - scaler\ \ Factor \geq 3\}$$

$$Timer\ \ Period = \frac{1}{Clock\ \ Source\ \ Frequency} \times \frac{1}{\Pr e - scaler\ \ Factor} \times (TMCNT + 1)\ [\sec] \qquad \{\Pr e - scaler\ \ Factor < 3\}$$

Timer Period Example :
- Clock Source Frequency : 12MHz System Clock
- Pre-scaler Factor : 1 / 1024
- Timer Counter Value (TMCNT) : 1000

=> 1/12MHz X 1024 X 1000 = 85.333msec = 11.718Hz

Following registers should be configured to run a timer counter.
- TPxCON : decide the clock input of pre-scaler. Also, it is used to clear pre-scaler.
- TMxCON's TMOD : decides the mode of Timer Counter
- TMxCON's WAVE: decide whether output or not the clock of timer counter period.
- TMxCON's PFSEL: decide the clock to be used for Timer Counter
- TMxCON's TMEN: Enable Timer Counter
- TMxCNT: Decide the maximum counter value of Timer Counter

Following procedure is required to run a Timer Counter.
- Set TPxCON
- Set TMxCNT
- Set TMxCTR
- Set CNTCLR bit of TPxCTRL register if necessary

28.2.3 Pulse Width Modulation (PWM)

PWM is a controller to output pulse signals of programmer-defined duty and period.

PWM references clock generated by pre-scaler, and outputs the wave form of user defined period.

PWM output pulse is toggled whenever its 32bit counter value reaches PWM duty or PWM period register value. The number of outputs is limited by PWM pulse number register. When it reaches the limit, PWM interrupt raises. However, if there is no special hanldler for the interrupt, PWM will output continuously. therefore, timer interrupt should disable PWM to stop PWM pulse.

$$PWM\ \ Pulse\ \ Period = \frac{1}{Clock\ \ Source\ \ Frequency} \times \frac{1}{\Pr e - scaler\ \ Factor} \times (TMCNT)\ [\sec] \qquad \{\Pr e - scaler\ \ Factor \geq 3\}$$

$$PWM\ \ Pulse\ \ Period = \frac{1}{Clock\ \ Source\ \ Frequency} \times \frac{1}{\Pr e - scaler\ \ Factor} \times (TMCNT + 1)\ [\sec] \qquad \{\Pr e - scaler\ \ Factor < 3\}$$

PWM Period Example :
- Clock Source Frequency : 12MHz System Clock
- Pre-scaler Factor : 1 / 1024
- PWM Period Value(TMxCNT) : 10
- PWM Duty Value : 6

=> 1/12MHz X 1024 X 10 = 0.853msec = 1.171KHz

Following registers should be configured to run PWM.
- TPxCTRL: choose clock input of pre-scaler. Also, it can be used to clear pre-scaler.
- TMxCTRL's TMOD: decide PWM mode
- TMxCTRL's PWML: decide start level of PWM output
- TMxCTRL's PFSEL: decide clock of PWM
- TMxCTRL's TMEN: enable PWM
- TMxCNT: decide the period of PWM
- TMxDUT: decide the duty of PWM
- TMxPUL: decide the number of pulse outputs of PWM. If it reaches it limit, timer interrupt raises. However, it doesn't stop PWM pulse output.

Following procedure is required to run PWM.
- Set TPxCTRL
- Set TMxCNT
- Set TMxDUT
- Set TMxPUL
- Set CNTCLR of TPxCTRL register if necessary

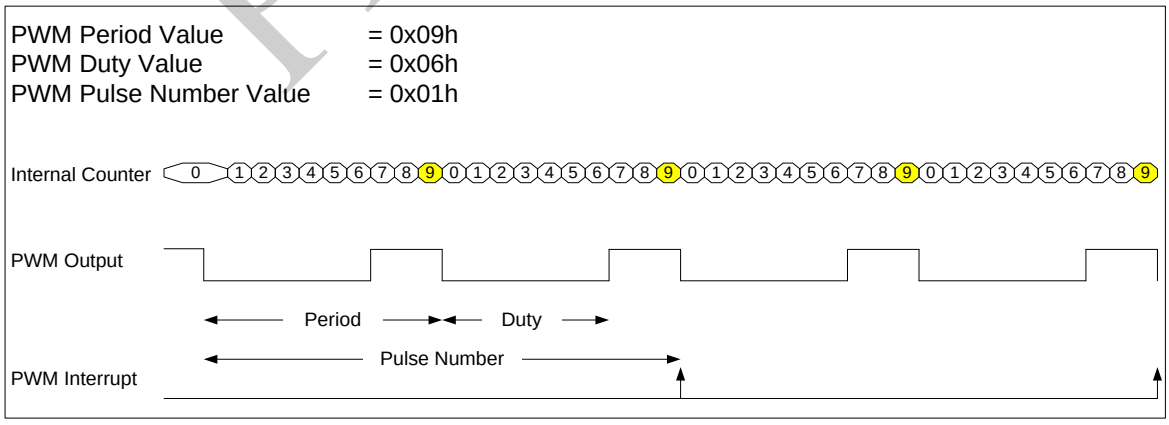


Figure 28-3 PWM Operation

28.2.4 Capture

Capture function measures the external output referencing the clock defined by pre-scaler.

Five kind of external periods can be measured: Low/High pulse, Low Pulse, High Pulse, Falling to Falling Period, Rising to Rising Period.

The first capture after enabling timer should be ignored because it is a transient value.

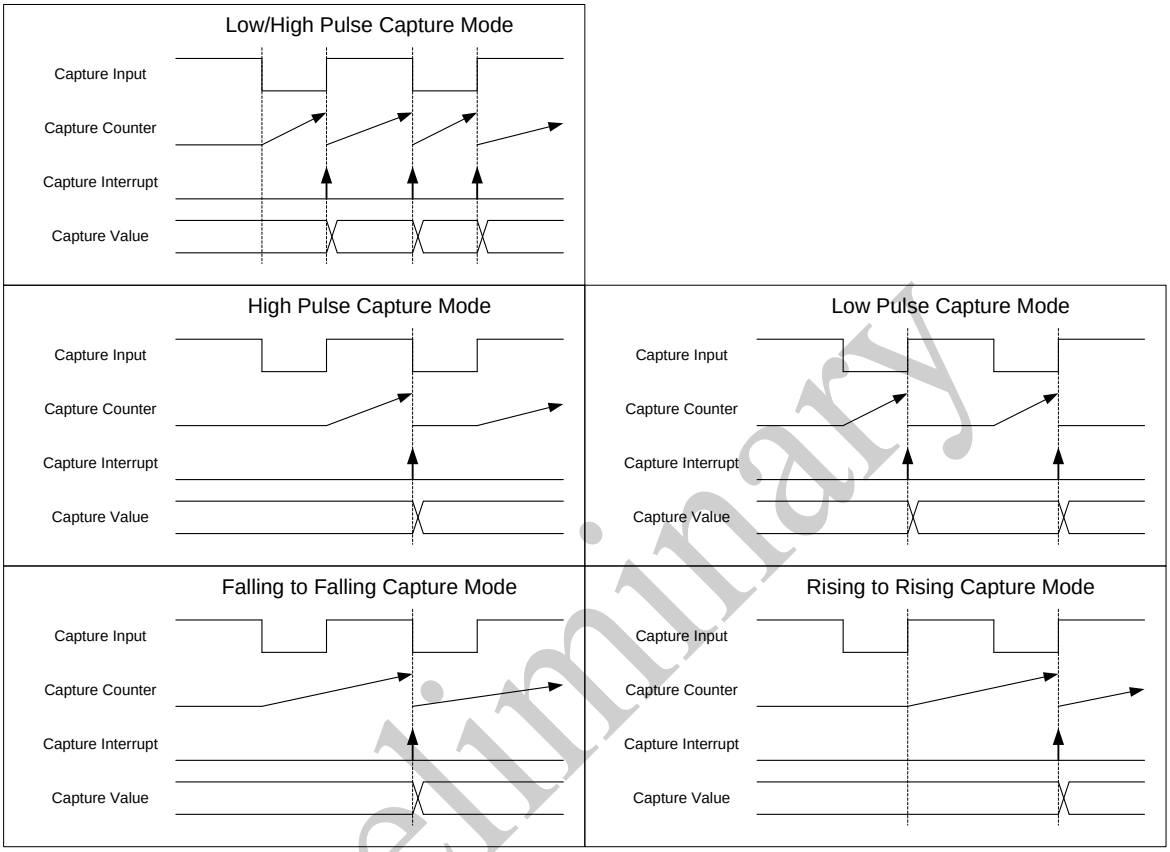


Figure 28-4 Capture Mode Operation

Calculating the period of captured pulses follows the below euqation.

$$Capture\ \ Signal\ \ Width\ \ Time = \frac{1}{Clock\ \ Source\ \ Frequency} \times \frac{1}{\Pr e - scaler\ \ Factor} \times (OCA + 1)\ \ [\sec]$$

Capture Time Example :
- Clock Source Frequency : 12MHz System Clock
- Pre-scaler Factor : 1 / 1024
- Capture Value : 9

=> 1/12MHz X 1024 X 10 = 0.853msec

To run in capture mode, following registers should be configured.

1. TPxCTRL: choose the clock input of pre-scaler. Also, can clear pre-scaler
2. TMxCTRL's TMOD: Change into capture mode
3. TMxCTRL's CAPMOD: decide the mode of pulse capturing
4. TMxCTRL's PFSEL: choose the clock for capturing
5. TMxCTRL's TMEN: enable capturing

Following procedure is required to run capturing.

1. Set TPxCTRL
2. Set TMxCTRL
3. Set the CNTCLR bit of TPxCTRL register if necessary
4. Check the period of capturing by reading TMxDUT
5. Check overflow by reading OVST of TMxCTRL register

28.3 Register Description

28.3.1 Timer Pre-scale Control Registers (TPxCTRL)

Address : 0xF400_3800 / 0xF400_3820 / 0xF400_3840 / 0xF400_3860

Bit	*R/W*	*Description*	*Default value*
31 : 2	R	Reserved	-
1	R/W	CNTCLR : Pre-scale Counter and Timer Counter Reset When this bit is "1", the Timer Pre-scale and Counter will be reset.	0
0	R/W	CLKSEL : Pre-scale Clock Selection 0 : System clock 1 : CAPx	0

*** CAPx assigned to each Timer channel

28.3.2 Timer Control Registers (TMxCTRL)

Address : 0xF400_3804 / 0xF400_3824 / 0xF400_3844 / 0xF400_3864

Bit	*R/W*	*Description*	*Default value*
31 : 16	R	Reserved	-
15 : 14	R/W	TMOD : Timer/Counter Mode 00 : Timer 01 : PWM 1x : Capture	00
13	R	Reserved	-
12	R	OVST : Capture Overflow Status bit	0
11	R	Reserved	0
10 : 8	R/W	CAPMOD : Capture Mode Selection 00x : Low/High Pulse Capture mode 010 : Low Pulse Capture mode 011 : High Pulse Capture mode 10x : Failing to Failing Period Capture mode 11x : Rising to Rising Period Capture mode	000
			1
6	R/W	PWMO : PWM Output One Period Generation 0 : Disable 1 : Enable	0
5	R/W	PWML : PWM Output Start Level 0 : Start Level is Low 1 : Start Level is High	0
4	R/W	TMOUT : Timer Wave Output Generation 0 : Disable 1 : Enable	0
3 : 1	R/W	PFSEL : Pre-scale Factor Selection 000 : 1/2 001 : 1/8 010 : 1/32 011 : 1/128 100 : 1/512 101 : 1/2048 110 : 1/8192 111 : 1/32768	111
0	R/W	TMEN : Timer/Counter or PWM Enable 0 : Disable 1 : Enable	0

*** PWM Output One Period Generation: Decide the number of period to be generated in PWM mode. After the number, PWM is automatically disabled.

*** Timer Wave Output Generation: Decide whether output or not the toggled wave form on every period in Timer mode.

28.3.3 Timer Counter / PWM Period Registers (TMxCNT)

Address : 0xF400_3808 / 0xF400_3828 / 0xF400_3848 / 0xF400_3868

Bit	R/W	Description	Default value
31 : 0	R/W	(Timer mode) - Write : Timer Counter Value - Read : Current Up-counter Value (PWM mode) - Read/Write : PWM Period Value	0xFFFF

28.3.4 Capture Counter Registers / PWM Duty Registers (TMxDUT)

Address : 0xF400_380C / 0xF400_382C / 0xF400_384C / 0xF400_386C

Bit	R/W	Description	Default value
31 : 0	R/W	(Capture mode) - Read : Result value of counting at the sampling period (PWM mode) - Read/Write : PWM Duty Value	0xFFFF

*** PWM Duty : First Halt Duty of PWM Pulse

28.3.5 PWM Pulse Count Registers (TMxPUL)

Address : 0xF400_3810 / 0xF400_3830 / 0xF400_3850 / 0xF400_3870

Bit	R/W	Description	Default value
31 : 0	R/W	(PWM mode) - Read/Write : PWM Pulse Number Value	0xFFFF

29 TWI (Two Wired Interface)

The AMAZON-II has a TWI controller to interface with general TWI bus. TWI has two signals: SCL and SDA.

29.1 Features

- Master transmitter mode
- Master receive mode
- Slave transmitter mode
- Slave receive mode
- Software programmable clock frequency
- Software programmable acknowledge bit
- Interrupt driven data-transfers
- Start/Stop/Repeated Start/Acknowledge generation
- Multi master operation

29.2 Block Diagram

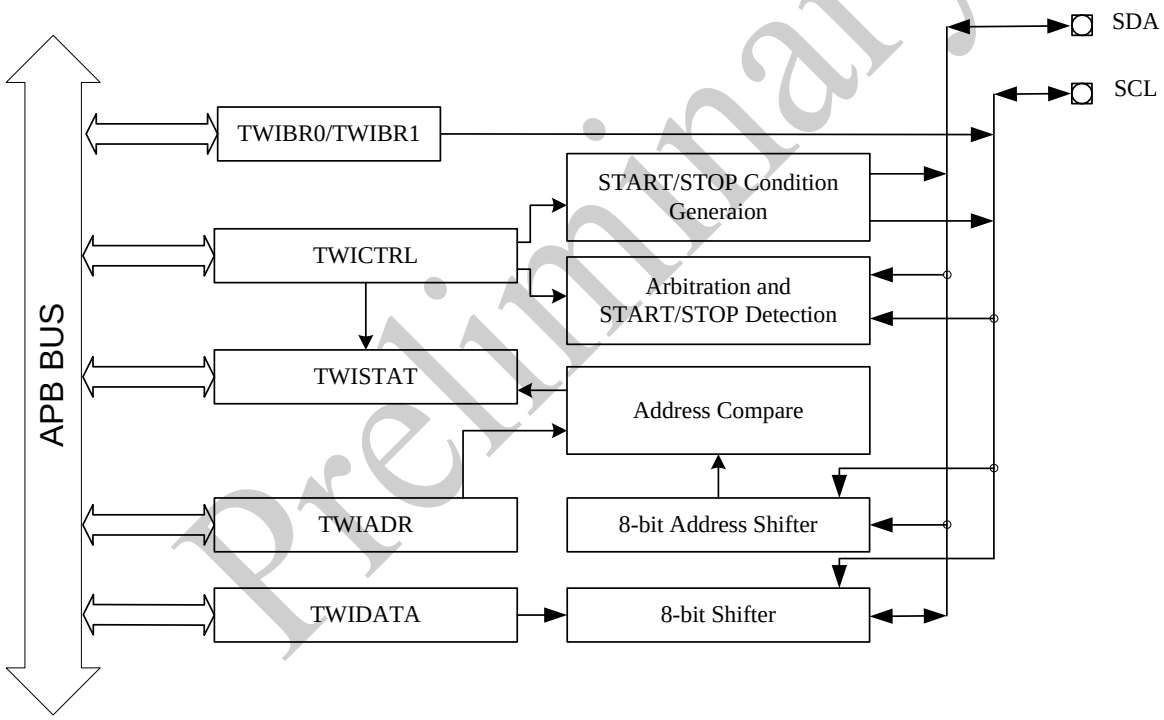


Figure 29-1 TWI Block Diagram

29.3 Function Description

29.3.1 DATA TRANSFER FORMAT

Every data on SDA line has 8bit width. The number of byte for a transfer is not limited. The first byte after start condition is address field. When TWI bus is in master mode, the master sends the address field Every bytes are followed by ACK bit. And always MSB bits are transferred first.

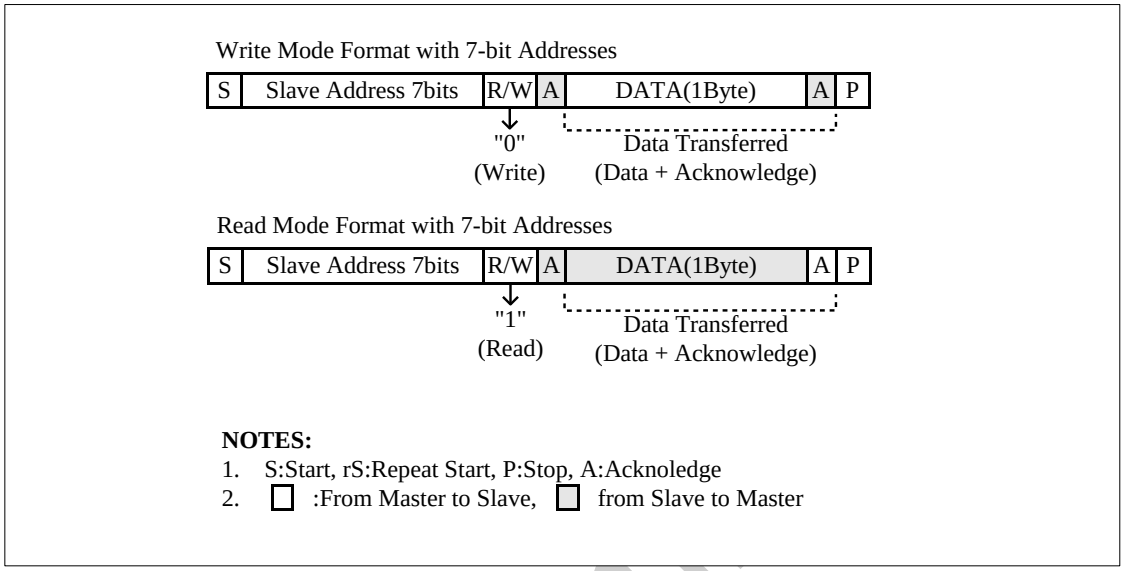


Figure 29-2 TWI-Bus Interface Data Format

29.3.2 START AND STOP CONDITION

Start condition initalizes a transfer, and stop condition finishes it. Start condition is the transition of SDA line from high-to-low during SCL line is kept in high. Stop condition is the transition of SDA line from low-to-high when SCL is high. If a start condition happens, TWI bus become busy. After a stop condition, TWI bus become free.

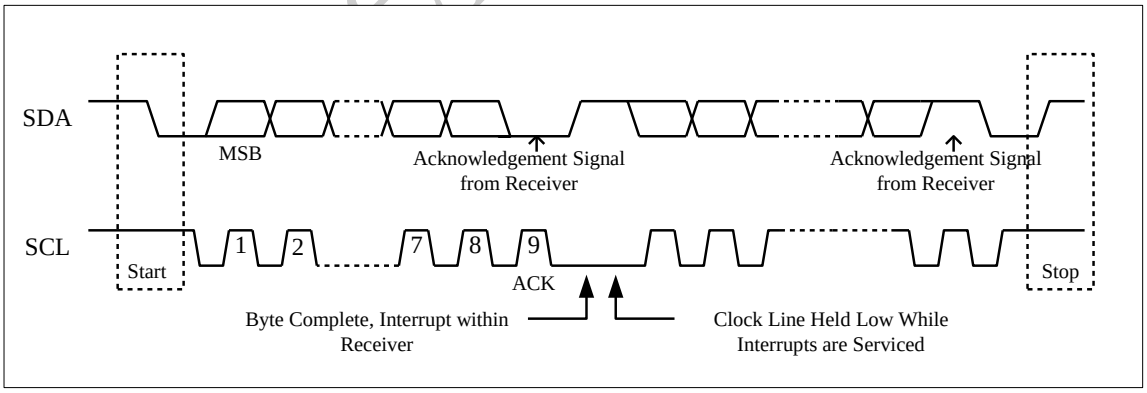


Figure 29-3 Data Transfer on the TWI-Bus

29.3.3 ACK SIGNAL TRANSMISSION

To finish a byte transfer, receiver should send a ACK bit to its sender. ACK pulse should happen at the ninth clock of SCL line. So we need 9 clocks to transfer a byte. Master should generate clock pulses fot ACK bit reception.

Sender should release SDA line to receive a ACK clock pulse. Receiver should should lower SDA line at ninth SCL period to change SDA line into “low”.

Software can set ACK bit can be ACK or NACK by setting. TXACK bit of control register.

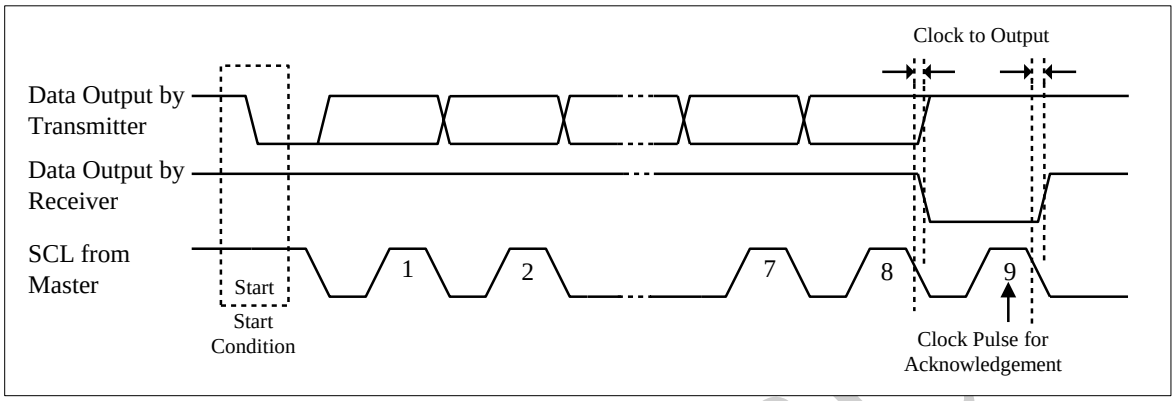


Figure 29-4 Acknowledgement of TWI

29.3.4 READ-WRITE OPERATION

In sending operation mode, TWI bus interface should wait until data shift register become ready after transfering data. Until data writing completes, SCL line will be kept low. SCL is released after new data is written in shift register.

When interruption is enabled, TWI raises interrupt after transfering current data.CPU writes new data into buffer after handling the interrupt request.

In receiving mode, TWI bus waits until TWI bus reads data after receiving data . During the reading, SCL is kept “low”. SCL is released after new data is read.

When interruption is enabled, TWI raises interrupt when data is received. The interrupted CPU reads the data.

29.3.5 BUS ARBITRATION PROCEDURES

Prevents multiple masters from controlling bus at the same time. If a master which sent high signal on SDA line senses other master's low level SDA signal the first master recognize that multiple masters are on bus, and stops its transfer.

When two devices become master mode at the same time, to say master 1 and master 2, the SCL line is synchronized as following clock wave form.

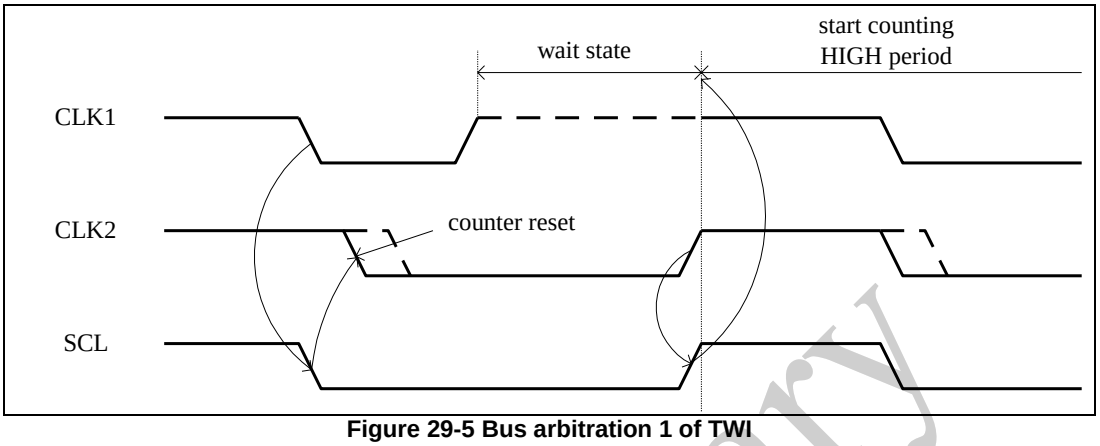


Figure 29-5 Bus arbitration 1 of TWI

In the above situation, either device 1 or device 2 will have priority depending on SDA line value as shown in the next diagram

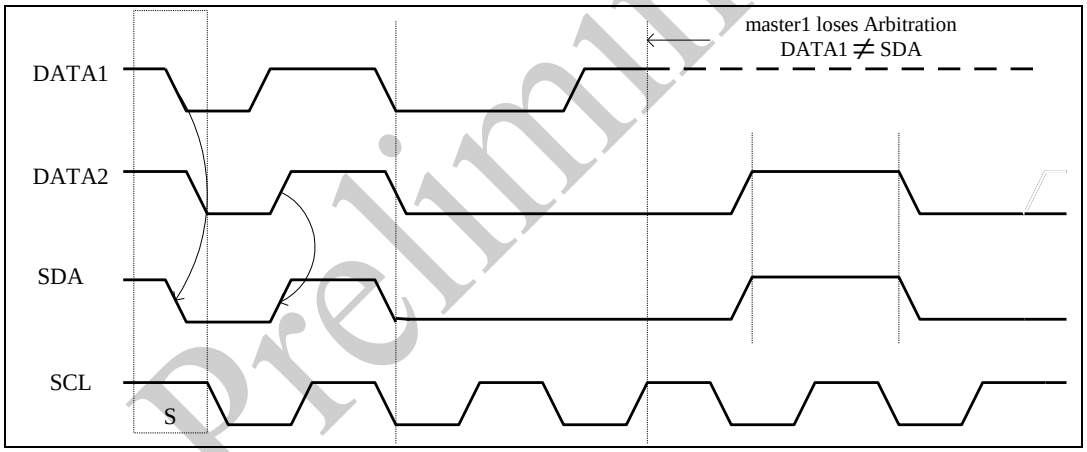


Figure 29-6 Bus arbitration 2

29.3.6 ABORT CONDITIONS

29.3.6.1 With arbitration

If MSTR bit of TWICTRL register is cleared, stop condition is generated.
No Ack generates stop condition. That is to say,SDA signal is not “low” under ACK period.

29.3.6.2 Without arbitration

Arbitration takes away control and clears MSTR bit, however, stop condition is not generated. SCL clock lasts until a byte transfer finishes, and SDA become “high”.

29.3.7 Operational Flow Diagrams

29.3.7.1 TWI initialization

First, TWI should be initialized.

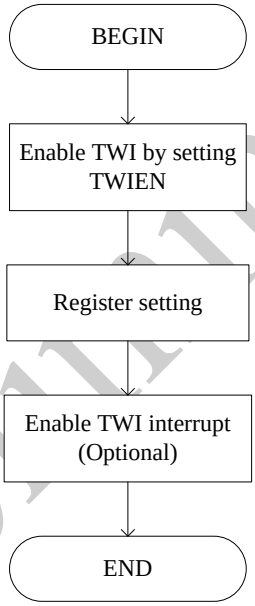


Figure 29-7 TWI Initialization Flow Char

29.3.7.2 Master Transmit / Receive

Below is the flow chart of TWI transmission and reception. For reception, additional steps are required. First, ACK bit should be set NO ACK upon the last data. This is to notify slave that master has sent its last data. Inaddition, dummy reading of TWIDATA register is required to generate SCL clock.

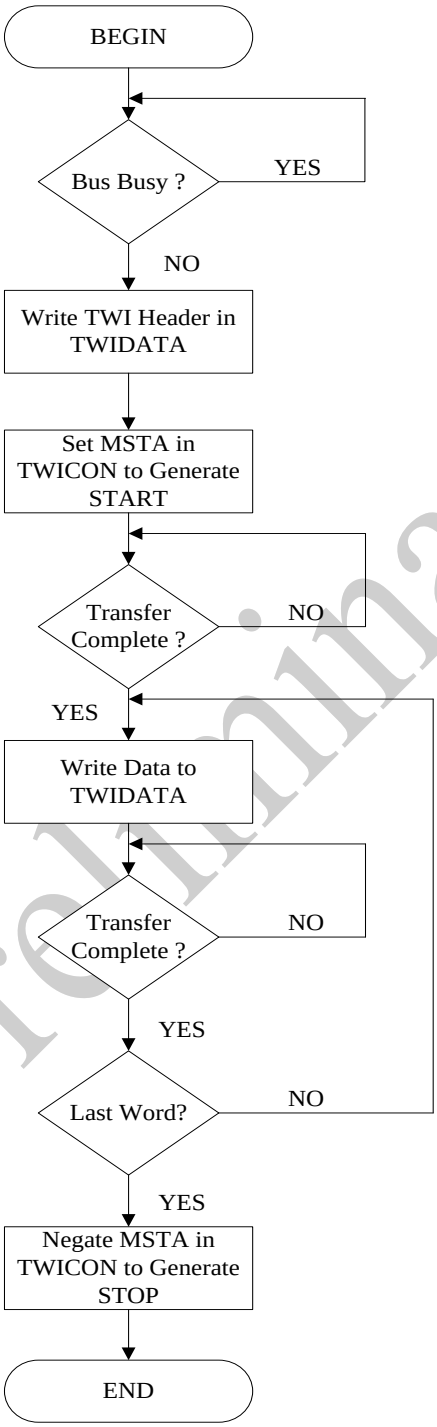


Figure 29-8 Master Transmit Flow Char

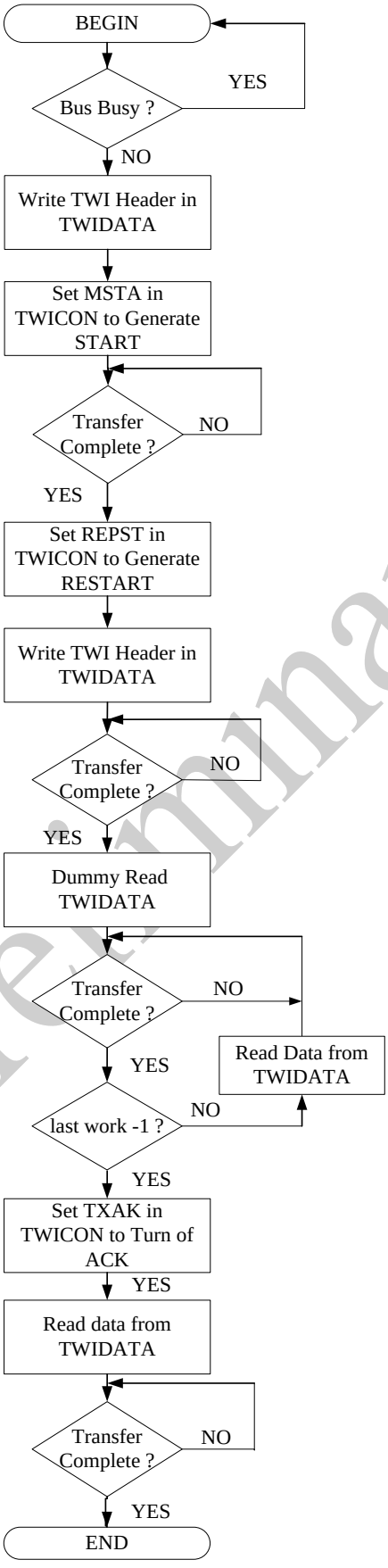


Figure 29-9 Master Receive Flow Char

29.3.7.3 Slave Mode (Polling mode)

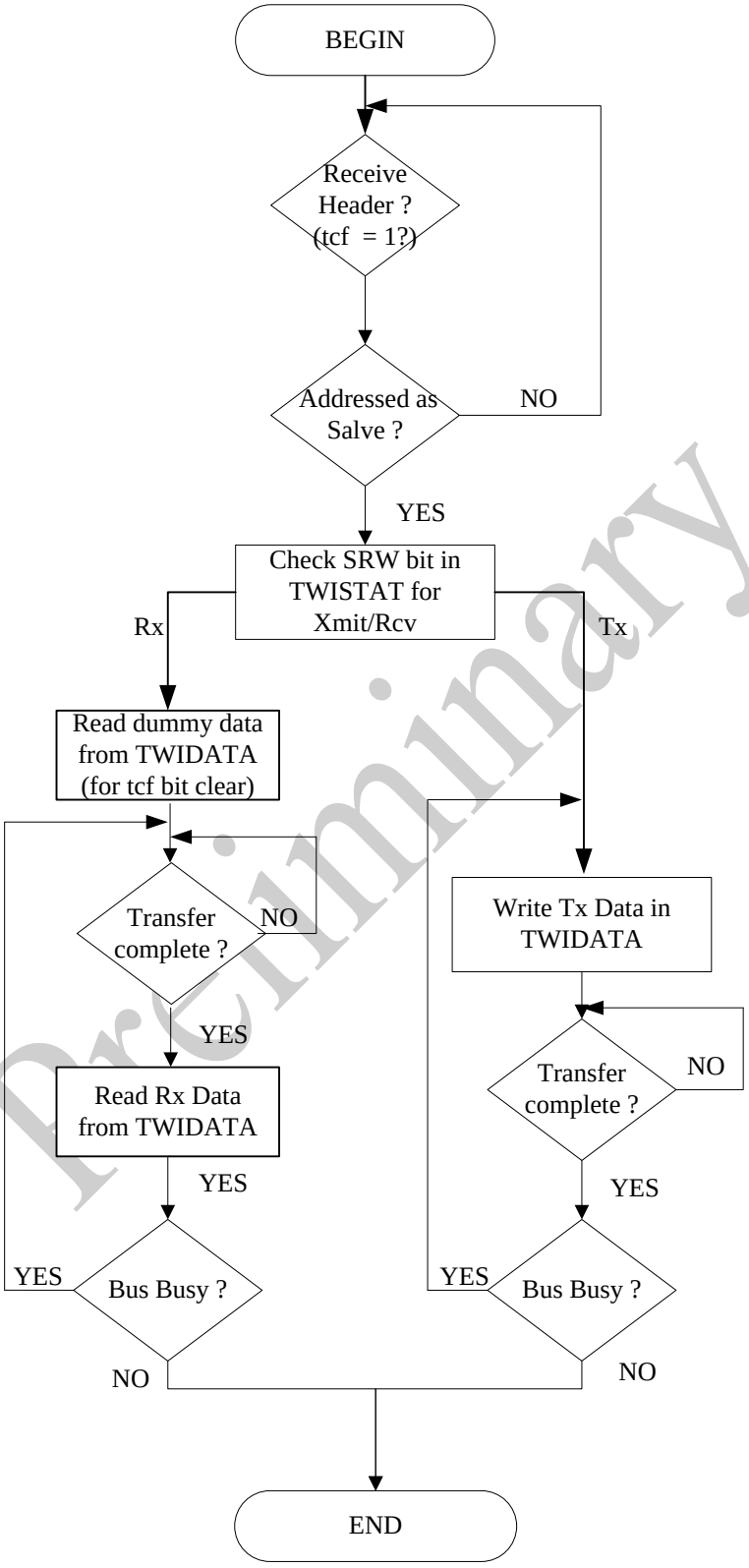


Figure 29-10 Slave Mode Flow Chart (Polling)

29.3.7.4 Slave Mode (Interrupt mode)

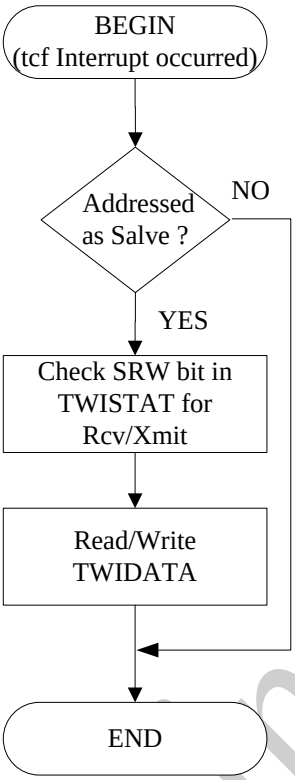


Figure 29-11 Slave Mode Flow Chart (Interrupt)

29.4 Register Description

29.4.1 TWI Control Register (TWICTRL)

Address : 0xF400_4000

Bit	*R/W*	*Description*	*Default value*
31 : 8	R	Reserved.	-
7	RW	TWIEN : TWI Controller Enable. For TWI transmission and reception, this bit should be set first. 0: Disable 1: Enable	0
6	R	Reserved.	-
5	RW	TWIMOD : Master/Slave Mode Select. When it toggles from 0 to 1, TWI enters into master mode, and START condition is generated. When it is cleared (1 to 0), STOP condition is generated, and TWI enters into slave mode. Though cleared, if TWI lost control right, STOP condition is not generated. 0: generates STOP condition 1: generates START condition	0
4	RW	TWITR : Transmit/Receive Mode Select. Decide operation in Master Mode 0: TWI Master receives 1: TWI Master transmits	0
3	RW	TWIAK : Transmit Acknowledge Enable. Decide SDA line value during ACK period. If it is in master receive mode and transmitting its last byte, NO ACK means that it is the last data transmission. After the last transmission, NO ACK generates STOP condition. 0: ACK bit = “0” – ACK (acknowledge) 1: ACK bit = “1” – NO ACK (no acknowledge)	0
2	RW	REPST : Repeated Start. If this be is set (=1) and TWI controller is in master mode, repeated START condition is generated. It is cleared after the repeated START condition is generated, 0: N/A	0

		1: generates repeated START condition	
1	R/W	TCIE : Transfer complete Interrupt enable bit Decide signaling interrupt or not when byte-unit transmission completes 0: Disable 1: Enable	0
0	R/W	LSTIE : Lost arbitration Interrupt enable bit Decide signaling interrupt or not when TWI lost its transmission write in master mode. 0: Disable 1: Enable	0

29.4.2 TWI Status Register (TWISTAT)

Address : 0xF400_4004

Bit	*R/W*	*Description*	*Default value*
31 : 10	R	Reserved.	-
9	RW	TXEMPTY : TX Buffer Empty. Represent the status of transmitting buffer. This bit can be written when it is 0. 0: TX buffer has data to transmit 1: TX buffer is empty	1
8	RW	RXFULL : RX Buffer Full. Represent the status of receiving buffer. This bit can be written when it is 1. 0: RX buffer is empty 1: RX buffer has data to be read	0
7	R	TWIDT : Data Transferring Bit. Set whenever a byte is transmitted, and cleared when TWIDATA register is read or written. Also, writing “1” clears this bit. 0: byte is being transmitted 1:byte transmission completed	0
6	R	TWIAS : Addressed as Slave Bit. When its address and received address coincide, TWI controller become slave. This bit is cleared when TWICON register is written or when STOP condition happens. 0: Address doesn’t coincides 1: Addresses coincides	0
5	R	TWIBUSY : Bus Busy Bit. Represent the status of TWI bus. Set by START condition and cleared by STOP condition. Also, writing “0” clears this bit. 0: Bus is in idle status 1: Bus is in busy status	0
4	RW	TWILOST : Lost Arbitration Bit. This bit is set when bus loses its control in master mode. Software can clear this bit by writing “1” to this bit. 0: Lost arbitration doesn’t happen 1: Lost arbitration happen	0
3	R	TWISRW : Slave Read/Write Bit. Represent transmit or receive mode in slave mode. 0: Slave receive mode 1: Slave transmit mode	0
2	R	Reserved.	-
1	RW	RSF : Repeated start flag Represent whether repeated START condition has happened or not. Set when repeated START condition happens, and cleared when STOP condition happens. Also, writing “1” when this bit is set will clear this bit. 0: Repeated START condition didn’t happen, or STOP condition happened. 1: Repeated START condition has happened.	0
0	R	TWIRXAK : Received Acknowledge Bit. Represent SDA line value during ACK period. 0: Acknowledge received 1: No Acknowledge received	1

29.4.3 TWI Address Register(TWIADR)

Address : 0xF400_4008

Bit	*R/W*	*Description*	*Default value*
31 : 8	R	Reserved.	-
7: 0	RW	(At only slave mode) [7:1] = Slave Address [0] = Not mapped	0x00

29.4.4 TWI Data Register (TWIDATA)

Address : 0xF400_400C

Bit	R/W	Description	Default value
31 : 8	R	Reserved.	-
7 : 0	RW	TWI data : Represent TWI data Write – written data or the address of accessing device Read – received data	0x00

29.4.5 TWI Baud-Rate 0 Register (TWIBR0)

Address : 0xF400_4010

Bit	R/W	Description	Default value
31 : 4	R	Reserved.	-
7 : 0	RW	Baud-rate 0 Value. TWIBR0 ≥ 3	0x0F

29.4.6 TWI Baud-Rate 1 Register (TWIBR1)

Address : 0xF400_4014

Bit	R/W	Description	Default value
31 : 9	R	Reserved.	-
8 : 0	RW	Baud-rate 1 Value.. TWIBR1 ≥ 0	0xFF

$$TWIBR0 = f_{PCLK} \times 700ns + 3$$

$$SCL = \frac{f_{PCLK}}{(2TWIBR1 + TWIBR0 + 7)}$$

$$TWIBR1 = \frac{f_{PCLK}}{2SCL} - \frac{TWIBR0 + 7}{2}$$

* f_{PCLK} = AMBA APB clock frequency

*SCL = TWI transmission rate

ex) If APB clock is 50MHz and TWI transmission rate is 400Kbps, (f_{PCLK} = 50MHz, SCL = 400Kbps)

$$TWIBR0 = 50MHz \times 700ns + 3 = 50 \times 10^{6} \times 700 \times 10^{-9} + 3 = 38$$

$$SCL = \frac{f_{PCLK}}{(2TWIBR1 + TWIBR0 + 7)} \Rightarrow 400Kbps = \frac{50MHz}{(2TWIBR1 + 38 + 7)} \Rightarrow 400 \times 10^{3} = \frac{50 \times 10^{6}}{(2TWIBR1 + 45)}$$

<Baud-rate Register Setting Reference Table>

f_{PCLK}	TWIBR0	TWIBR1			
		400Kbps	300Kbps	200Kbps	100Kbps
48Mhz	37(0x25)	38(0x26)	58(0x3A)	98(0x62)	218(0xDA)
24Mhz	20(0x14)	17(0x11)	27(0x1B)	47(0x2F)	107(0x6B)
12Mhz	12(0xC)	6(0x6)	11(0xB)	21(0x15)	51(0x33)
6Mhz	7(0x7)	1(0x0)	3(0x3)	8(0x8)	23(0x17)
11.2896Mhz	11(0xB)	5(0x5)	10(0xA)	19(0x13)	48(0x30)
5.6448Mhz	7(0x7)	0(0x0)	3(0x3)	7(0x8)	21(0x16)

* Above table can bear some errors.

30 SPI (Serial Peripheral Interface)

The AMAZON-II includes SPI which exchanges data with external devices and other CPUs through synchronized serial bus. This SPI is compatible with the SPI of M16HC11, M68HC05, and MC68HC16 series of Motorola, and supports full duplex 3-wire or half duplex 2-wire transmission.

For high speed SPI transmission, the SPI of the Amzon2 has FIFO of 8 bytes. The FIFO allows several Mbps of transmission rate without imposing overhead on CPU.

The SPI of the Amzon2 supports both master mode and slave mode.

30.1 Features

- Full duplex mode. Three-wired synchronous Transfer
- Master or Slave Operation
- Programmable clock polarity and phase
- End of transmission interrupt flag
- Write collision flag protection
- Master-master mode fault protection capability
- 8Bytes FIFO

30.2 Block Diagram

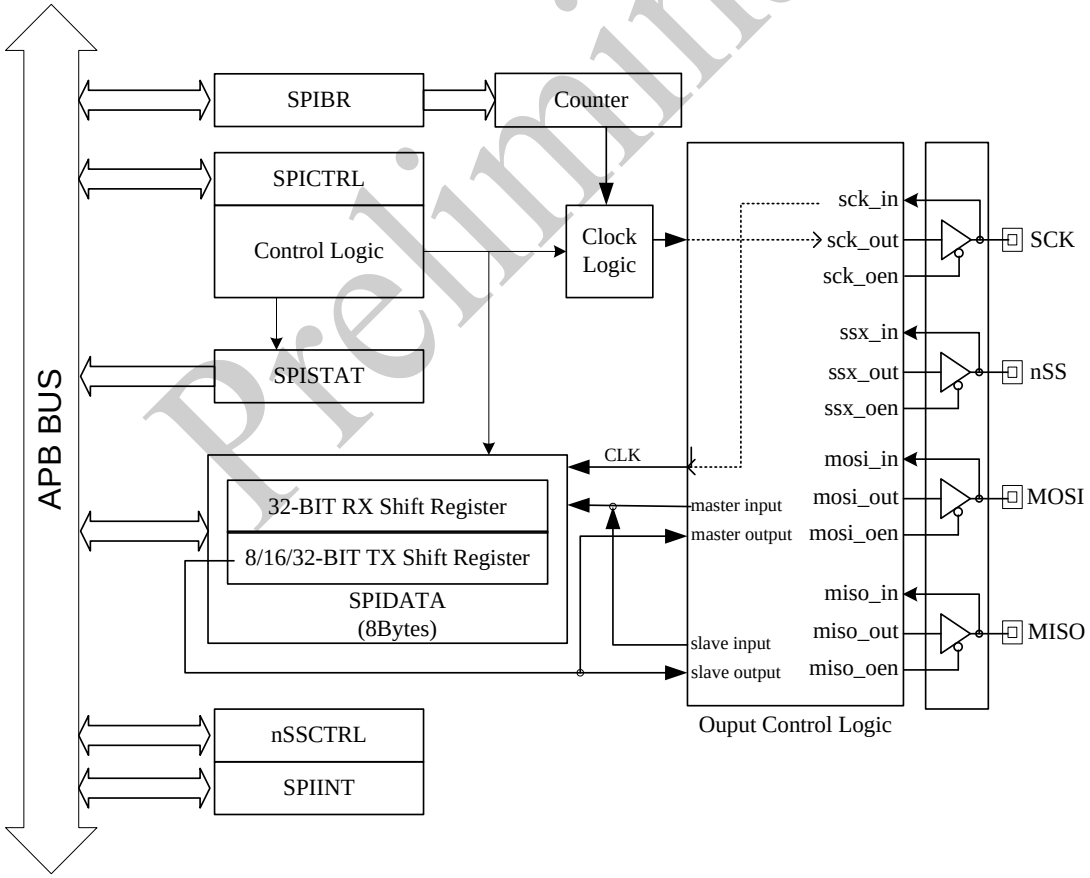


Figure 30-1 SPI Block Diagram

30.3 Function Description

The clock control circuit of the SPI can adjust its polarity and protocol so as to communicate with most of synchronized serial peripherals. When the SPI is set as a master, it can generate 256 various serial clocks in software.

The SPI can transmit and receive data at the same time. Sampling and shifting of two serial data lines are synchronized by serial clock line. Slave select line(nSS) can choose which SPI device to use. Unselected SPI devices don't affect SPI bus. The nSS line can be used to notify conflict among multiple masters in master SPI mode.

Error detection circuit is used to connect processes. When shift register is written during transmission operation, it is a conflict. Multiple master mode failure detector disables output driver when more than one CPUs try to become bus master.

30.3.1 SPI Pins

SPI has four bi-directional pins: MISO, MOSI, SCK, and nSS. WOMP bit of SPI control register decides the output operation mode of each pins. Possible output operation modes are open drain and CMOS.

MSTR bit of SPI control register decides whether the SPI will operate as a master or a slave, and pins also follow the decision.

Table 30-1 SPI Pin Functions

Pin Name	*Mode*	*Function*
Master in, slave out(MISO)	Master	Provides serial data input to the SPI
	Slave	Provides serial data output from the SPI
Master out, slave in (MOSI)	Master	Provides serial output from the SPI
	Slave	Provides serial input to the SPI
serial clock(SCK)	Master	Provides clock output from the SPI
	Slave	Provides clock input to the SPI
Slave select(nSS)	Master	Output : Selects slave devices
	Slave	Input : chip select for SPI

30.3.2 SPI Operating Modes

SPI can become either master or slave. When itsCPU controls data transmission, its mode is master. On the other hand, when a external device controls the data transmission, its mode is slave. MSTR bit of control register decides the mode.

1 Master Mode

If the MSTR bit of SPICTRL is set, SPI operates as master mode. Master can initialize serial transmission, and doesn't respond to initialization from external side.

In master mode, MISO pin is used for serial data input, and MOSI pin is used for serial data output. Depending on application area, one or two of these can be used.

Following procedure is required to use SPI in master mode.

1. Set BAUD, CPHA, CPOL, SIZE, MSBF, and WOMP of SPICTRL register.
2. MSTR bit should be set for master mode.
3. Set SPIEN bit to enable SPI.
4. Enable slave device.
5. Write proper data on SPIDATA register to begin transmission.
6. When the transmission finishs, SPIF flag of SPISTAT register is set by hardware, and it raises interrupt request. SPIF flag will be cleared automatically after reading SPISTAT and read or write SPIDATA register.

Data transmission is synchronized with internal serial clock(SCK). CPHA and CPOL bits of SPICTRL register controls phase and polarity of the clock. The clock is used for both transmitting data into MOSI pin and latching data from MISO pin.

2 Slave Mode

If MSTR bit of SPICTRL register is set to "0", the SPI becomes slave mode. In slave, SPI cannot initialize serial transmission. Transmissions are only initialized by external bus master. The slave mode is used when there are multiple masters on SPI bus because only one device can become the bus master at a time.

In slave mode, MISO pin is used for serial data output, and MOSI pin is used for data input. Depending on its application area, one or both of these can be used. SCK is input serial clock, and nSS signal is required to become active.

Data register should be written for data transmission. In slave mode, SCK, MOSI, and nSS pin are input, and MISO pin is output. CPHA, CPOL, SIZE, MSBF, and WOMP should be written. MSTR bit should be cleared for slave mode. SPIEN should be set to enable SPI. In slave mode, BAUD value does not affect SPI's operation.

When SPIEN is set and MSTR is cleared, "LOW" status of nSS pin initialize the operation of slave mode. nSS pin is only input.

After transmitting a byte or a word, SPI sets SPIF flag. If SPIF is set when SPIE is "1", a interrupt request raises.

Transmission is synchronized with external SCK. CPHA and CPOL are used to latch data from MOSI pin or to decide clock edge of outgoing data through MISO pin.

30.3.3 SCK Phase and Polarity Control

Two bits of control register decide the phase and polarity of SCK. CPOL bit decides the polarity of the clock(high or low). CPHA bit decide the phase of transmission which affects the timing of transmission. The polarity and phase of master and slave should be same. However, in some cases, Master can communicate with slave with different polarity and phase by changing them during a transmission. This flexibility of SPI allows it direct connection with most of synchronized serial peripherals.

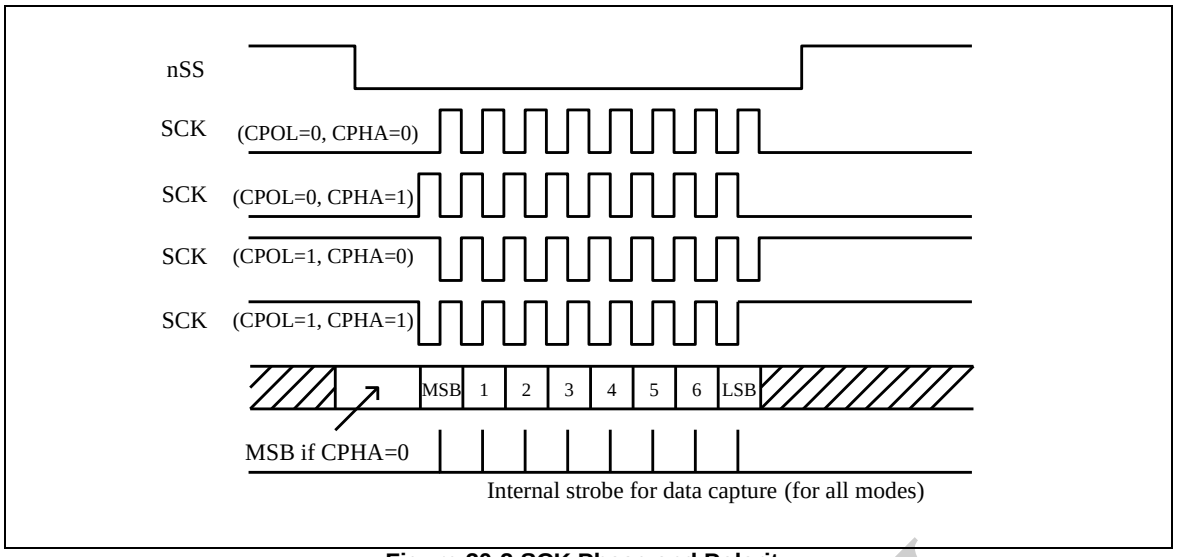


Figure 30-2 SCK Phase and Polarity

30.3.4 Data Transfer Timing

Following figure shows data transmission timing diagram when CPHA is '0' and MSB is comes first. It shows two form of SCK. One is when CPOL is '0', and the other is when CPOL is '1'. It can be a diagram of both master and slave because they share SCK, MISO, and MOSI lines. MISO signal is a output of slave, and MOSI signal is output of master. nSS signal is chip select.

If master write data on SPDR, transmission is initialized. Slave is initialized when nSS sees a falling edge. SCK signal remains inactive until the half period of SCK cycle.SPIF bit which represent the end of a transmission is set at the eighth SCK cycle. When CPHA is '0', nSS toggles from low to high after transmitting a byte. If a slave write on data register when nSS is low, write collision error raises.

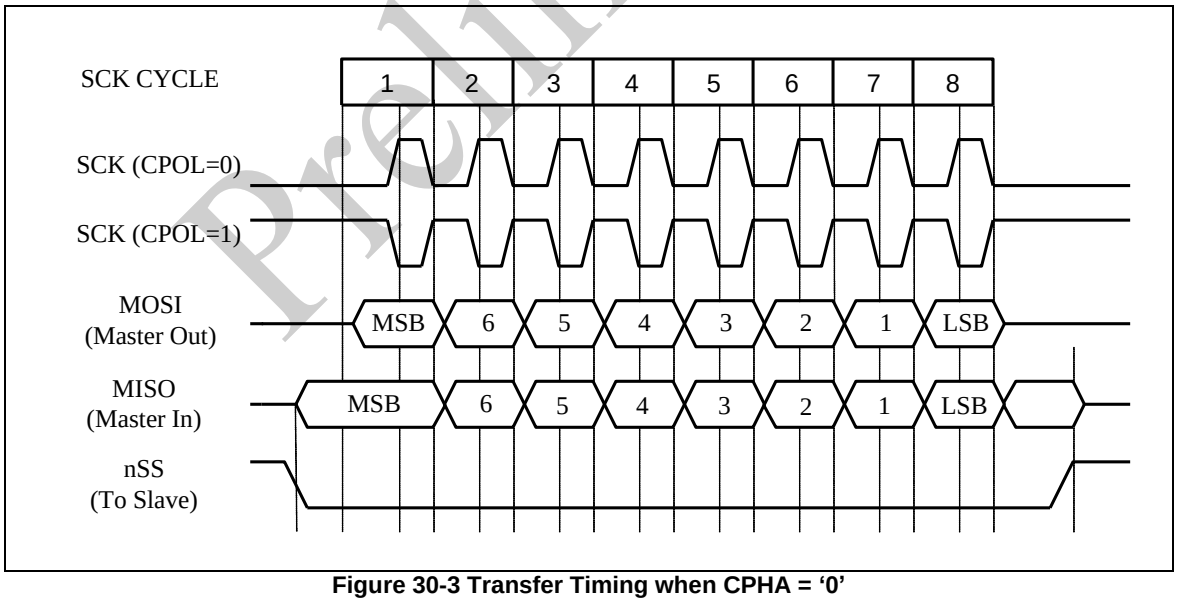


Figure 30-3 Transfer Timing when CPHA = '0'

The next figure is for CPHA='1'. SCK become inactive at the half period of the eighth cycle. SPIF bit is set at the end of the eighth SCK cycle. Because the last edge is generated at the middle of the eighth SCK cycle, slave finishes receving after samping the last data. nSS keeps "low" state during enough time after transmitting 1 byte.Thus, if CPU continuously sends data, nSS keeps low state.

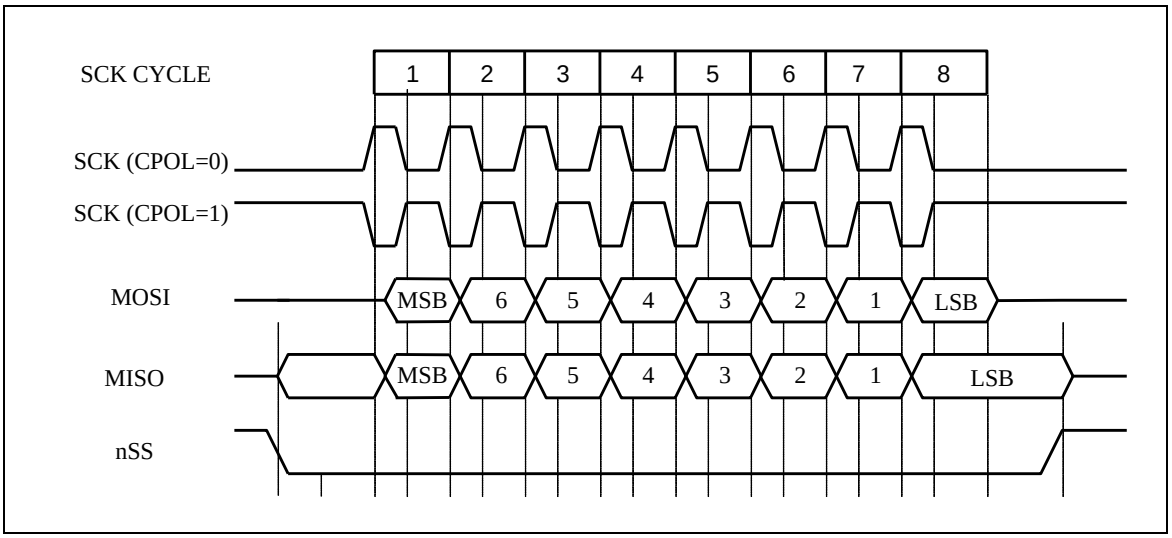


Figure 30-4 Transfer Timing when CPHA = '1'

30.3.5 SPI Serial Clock Baud Rate

SPI Baud rate can be set between 1 to 255 by writing SPBR register. In slave mode, SCK is therefore given by external SPI master; So, SPIBRR register value is ignored. However, maximum speed is limited by system clock.

$$SCK\ Baud\ Rate = \frac{f_{PCLK}}{2 \times (SPIBR + 1)}$$

or

$$SPIBR = \frac{f_{PCLK}}{2 \times SCK\ Baud\ Rate} - 1$$

30.3.6 Open-Drain Output for Wired-OR

Unless there are multiple SPI masters, SPI bus output doesn't need to support open-drain. When open-drain output is necessary, WOMP bit of SPICTRL register should be set. Pull-up register is necessary for each open-drain output line

30.3.7 Transfer Size and Direction

SPISIZE bit of SPICTRL register decide the transfer size of SPI: 8, 16, or 32bit. MSBF bit of SPICTRL register decides which bit to transfer first (MSB or LSB).

30.3.8 Write Collision

Write collision raises if one try to write SPIDATA register during a transmission.

30.3.9 MODE Fault

If mode fault error happens when SPI is set to master mode and nSS signal input line is asserted, MODF bit of SPISTAT is set. MODF can be set only under master mode, and it happens when other SPI device tries to become a master.

30.3.10 Interrupt

30.3.10.1 SPIF Interrupt

It is raised when both FIFO and TX shift register become empty, and this means SPI transmission is complete.

30.3.10.2 MODF Interrupt

It is raised when mode fault happens. Mode fault happens when more than one master try to transmit data.

30.3.10.3 nSS Interrupt

It is occurred when nSS port is changed.

30.3.10.4 TX_FIFO_FULL, TX_FIFO_EMPTY, RX_FIFO_FULL, RX_FIFO_EMPTY

TX_FIFO_FULL: Means the internal 8 byte FIFO became full. If more data are added to FIFO when it's full, data transmission will be corrupted.
TX_FIFO_EMPTY: Means every data in the FIFO are transmitted. However, because TX shift register can be not empty yet, so this interrupt doesn't mean SPI transmission is completed.
RX_FIFO_FULL: means RX_FIFO is full.
RX_FIFO_EMPTY: means RX_FIFO is empty.

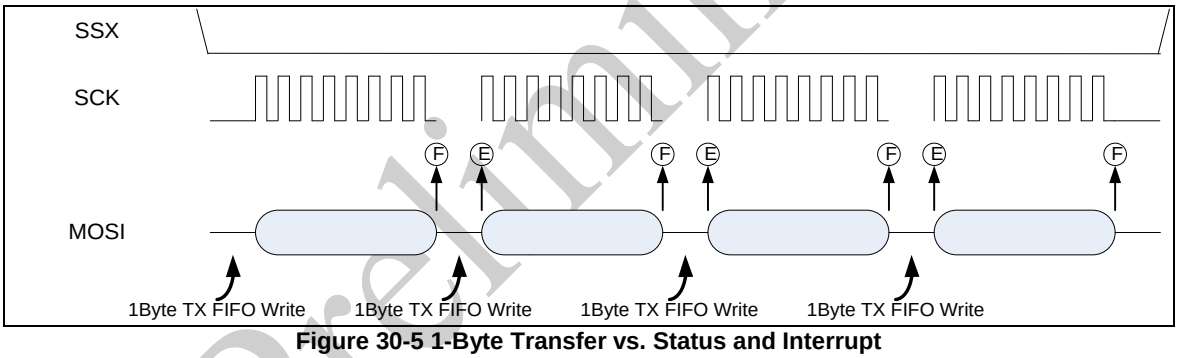


Figure 30-5 1-Byte Transfer vs. Status and Interrupt

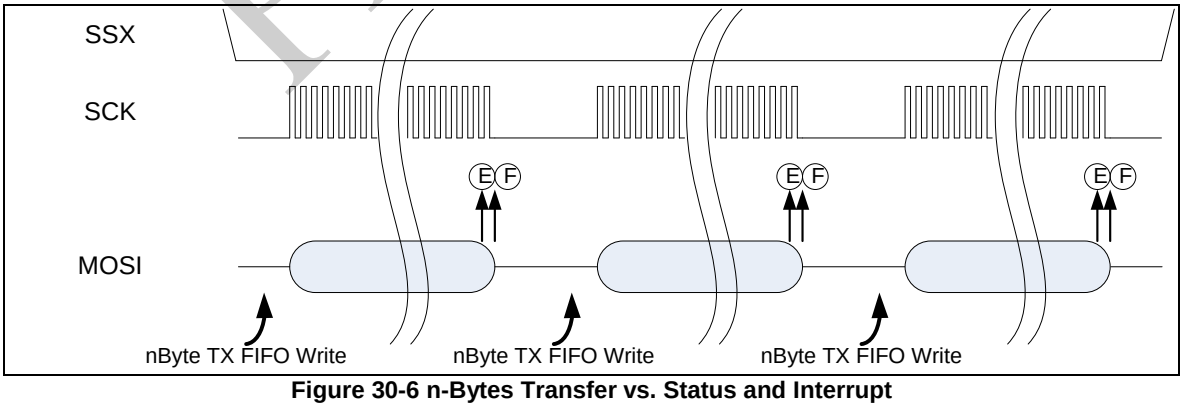


Figure 30-6 n-Bytes Transfer vs. Status and Interrupt

30.4 Register Description

30.4.1 SPI Control Register (SPICTRL)

Address : 0xF400_4C00 / 0xF400_4C40

Bit	R/W	Description	Default value
31 : 8	R	Reserved	-
7	R/W	SPIEN : SPI Enable 0 : SPI is disabled. 1 : SPI is enabled	0
6	R/W	WOMP : Wired-OR Mode for SPI Pins 0 : Outputs have normal CMOS drivers. 1 : Open-drain drivers	0
5	R/W	MSTR : Master/Slave Mode Select 0 : Slave operation 1 : Master operation	0
4	R/W	CPOL : Clock Polarity 0 : The inactive state value of SCK is logic level zero 1 : The inactive state value of SCK is logic level one.	0
3	R/W	CPHA : Clock Phase 0 : Data captured on the leading edge of SCK and changed on the trailing edge of SCK. 1 : Data is changed on the leading edge of SCK and captured on the trailing edge of SCK.	0
2	R/W	MSBF : Most Significant Bit First 0 : Serial data transfer starts with LSB. 1 : Serial data transfer starts with MSB.	0
1 : 0	R/W	SPISIZE : Transfer Data Size 00 : 8-bit data transfer. 01 : 16-bit data transfer. 10 : 32-bit data transfer.	0

30.4.2 SPI Baud Rate Register (SPIBR)

Address : 0xF400_4C04 / 0xF400_4C44

Bit	R/W	Description	Default value
31 : 8	R	Reserved.	-
7 : 0	R/W	Serial Clock Baud Rate $SCK = \frac{f_{PCLK}}{2 \times (SPIBR + 1)}$ Master Mode SCK ≤ System Clock / 2 Slave Mode SCK ≤ System Clock / 4	0xFF

30.4.3 SPI Status Register (SPISTAT)

Address : 0xF400_4C08 / 0xF400_4C48

Bit	R/W	Description	Default value
15 : 8	R	Reserved	-
7	R	SPIF : SPI Finished Flag 0 : SPI is not finished. 1 : SPI is finished.	0
6	R	WCOL : Write Collision 0 : No attempt to write to the SPDR happened during the serial transfer. 1 : Write collision occurred.	0
5	R	MODF : Mode Fault Flag 0 : Normal operation 1 : Another SPI node requested to become the network SPI master while the SPI was enabled in master mode	0
4	R	nSS : Slave Select Flag 0 : Current Value of nSS port is low 1 : Current Value of nSS port is high	0
3	R	STXF : TX FIFO Full Status bit 0 : FIFO_TX is not full 1 : FIFO_TX is full	0
2	R	STXE : TX FIFO Empty Status bit 0 : FIFO_TX is not empty 1 : FIFO_TX is empty	0
1	R	SRXF : RX FIFO Full Status bit 0 : FIFO_RX is not full 1 : FIFO_RX is full	0
0	R	SRXE : RX FIFO Empty Status bit 0 : FIFO_RX is not empty 1 : FIFO_RX is empty	0

30.4.4 SPI Data Register (SPIDATA)

Address : 0xF400_4C0C / 0xF400_4C4C

Bit	R/W	Description	Default value
31 : 0	R/W	SPI Data At 32-bit transfer mode - MSB of Data is SPDR[31] At 16-bit transfer mode - MSB of Data is SPDR[15] At 8-bit transfer mode - MSB of Data is SPDR[7] LSB of Data (received or transmit) is SPDR[0] in any transfer mode	0x0000_0000

30.4.5 SPI nSS Control Register (nSSCTRL)

Address : 0xF400_4C10 / 0xF400_4C50

Bit	R/W	Description	Default value
31 : 1	R	Reserved	-
0	RW	nSSCON : nSS Output Level	1

30.4.6 SPI Interrupt Mask Register (SPIINT)

Address : 0xF400_4C14 / 0xF400_4C54

Bit	R/W	Description	Default value
31 : 8	R	Reserved	-
7	RW	SPIFE : SPIF Interrupt en/disable SPIF Interrupt occurs when transfer has completed. 0 : SPIF interrupt is disabled 1 : SPIF is enabled	0
6	RW	MODFE : MODFI Interrupt en/disable MODFI Interrupt occurs when two more master use data line. 0 : MODFI interrupt is disabled 1 : MODFI is enabled	0
5	R	Reserved	0
4	RW	nSSEN : nSS Interrupt en/disable nSS Interrupt occurs when nSS signal has changed. 0 : nSS Interrupt is disabled 1 : nSS Interrupt is enabled	0
3	RW	STXFE : FIFO_TX_FULL Interrupt en/disable FIFO_TX_FULL Interrupt occurs when FIFO_TX is full 0 : FIFO_TX_FULL Interrupt is disabled 1 : FIFO_TX_FULL Interrupt is enabled	0
2	RW	STXEE : FIFO_TX_EMPTY Interrupt en/disable FIFO_TX_EMPTY Interrupt occurs when FIFO_TX is empty 0 : FIFO_TX_EMPTY Interrupt is disabled 1 : FIFO_TX_EMPTY Interrupt is enabled	0
1	RW	SRXFE : FIFO_RX_FULL Interrupt en/disable FIFO_RX_FULL Interrupt occurs when FIFO_RX is full 0 : FIFO_RX_FULL Interrupt is disabled 1 : FIFO_RX_FULL Interrupt is enabled	0
0	RW	SRXEE : FIFO_RX_EMPTY Interrupt en/disable FIFO_RX_EMPTY Interrupt occurs when FIFO_RX is empty 0 : FIFO_RX_EMPTY Interrupt is disabled 1 : FIFO_RX_EMPTY Interrupt is enabled	0

30.4.7 SPI nSS Control Register (nSSCTRL)

Address : 0xF400_4C10 / 0xF400_4C50

Bit	R/W	Description	Default value
31 : 1	R	Reserved	-
0	RW	nSSCON : nSS Output Level	1

30.4.8 SPI Interrupt Mask Register (SPIINT)

Address : 0xF400_4C14 / 0xF400_4C54

Bit	R/W	Description	Default value
31 : 8	R	Reserved	-
7	RW	SPIFE : SPIF Interrupt en/disable SPIF Interrupt occurs when transfer has completed. 0 : SPIF interrupt is disabled 1 : SPIF is enabled	0
6	RW	MODFE : MODFI Interrupt en/disable MODFI Interrupt occurs when two more master use data line. 0 : MODFI interrupt is disabled 1 : MODFI is enabled	0
5	R	Reserved	0
4	RW	nSSEN : nSS Interrupt en/disable nSS Interrupt occurs when nSS signal has changed. 0 : nSS Interrupt is disabled 1 : nSS Interrupt is enabled	0
3	RW	STXFE : FIFO_TX_FULL Interrupt en/disable FIFO_TX_FULL Interrupt occurs when FIFO_TX is full 0 : FIFO_TX_FULL Interrupt is disabled 1 : FIFO_TX_FULL Interrupt is enabled	0
2	RW	STXEE : FIFO_TX_EMPTY Interrupt en/disable FIFO_TX_EMPTY Interrupt occurs when FIFO_TX is empty 0 : FIFO_TX_EMPTY Interrupt is disabled 1 : FIFO_TX_EMPTY Interrupt is enabled	0
1	RW	SRXFE : FIFO_RX_FULL Interrupt en/disable FIFO_RX_FULL Interrupt occurs when FIFO_RX is full 0 : FIFO_RX_FULL Interrupt is disabled 1 : FIFO_RX_FULL Interrupt is enabled	0
0	RW	SRXEE : FIFO_RX_EMPTY Interrupt en/disable FIFO_RX_EMPTY Interrupt occurs when FIFO_RX is empty 0 : FIFO_RX_EMPTY Interrupt is disabled 1 : FIFO_RX_EMPTY Interrupt is enabled	0

31 Electrical Characteristic

31.1 Absolute Maximum Ratings

Parameter	Symbol	Min		Max	Unit
Core supply voltage range	VVDD	-0.5		1.6	V
I/O supply voltage range	VDVDD	-0.5		3.8	V
Voltage range at PAD	VPAD	-0.5		VDVDD + 0.5	V
Operating temperature range	T_A	-40		85	˚C

31.2 Recommended Operating Conditions

Parameter	Symbol	Min	NOM	Max	Unit
Core supply voltage	VVDD	1.08	1.2	1.32	V
I/O supply voltage	VDVDD	2.97	3.3	3.63	V
Junction temperature	T_J	-40	25	125	˚C
Voltage at PAD	VPAD	0		VDVDD	V
High-level input voltage at PAD	VIH	0.7 VDVDD		-	V
Low-level input voltage at PAD	VIL	-		0.2 VDVDD	V

31.3 DC Characteristics

Parameter	Symbol	Min	NOM	Max	Unit
Low level output current @ VOL =0.4V 8mA Drive strength	IOL	8.4	15.6	23.9	mA
High level output current @ VOH = VDVDD -0.4V 8mA Drive strength	IOH	9.14	14.0	19.3	mA

31.4 Pull Resistors

Parameter	Value	Unit
Pull-up	113	kΩ
Pull-down	83	kΩ

31.5 USB PHY Recommended Operating Conditions

Parameter	Symbol	Min	NOM	Max	Unit
High-level input voltage at DPOS/DNEG	VIH	1.30	1.55	1.90	V
Low-level input voltage at DPOS/DNEG	VIL	0.90	1.13	1.40	V
DPOS capacitance(1)		-	4.588	-	pF
DNEG capacitance(1)		-	4.332	-	pF
Output Driver Impedance(2) (Output high, PMOS driver)		5.5	9.5	13.5	Ω
Output Driver Impedance(2) (Output low NMOS driver)		5.8	9.3	13.5	Ω

Capacitances were measured under typical conditions:1.2V/3.3V, typical/typical and 25˚C
Based on measured silicon

31.6 USB PHY Switching Characteristics Over Recommended Operating Conditions

Parameter	Symbol	LOW SPEED			FULL SPEED			Unit
		Min	NOM	Max	Min	NOM	Max	
Rise time, DPOS/DNEG	t_R	70	85	140	4.7	8.5	15.6	ns
Fall time, DPOS/DNEG	t_F	65	87	130	5.9	8.7	21.1	ns
Crossover Rise Voltage		1.47	1.63	2.00	1.56	1.71	1.88	V
Crossover fall Voltage		1.50	1.65	2.10	1.62	1.73	1.92	V

31.7 PLL Electrical Specification

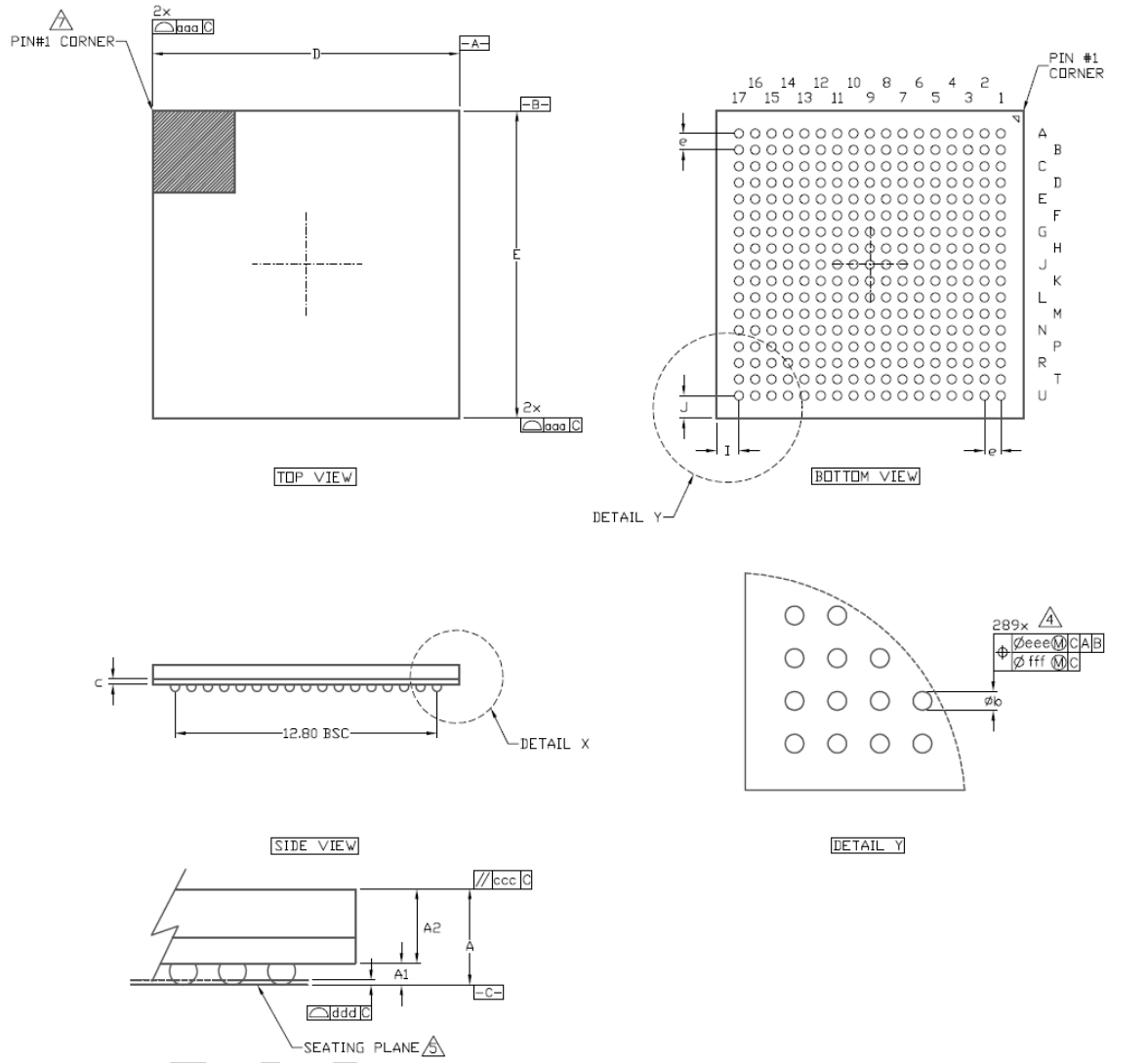
Parameter	Symbol	Min	NOM	Max	Unit
Input frequency	FREF	5		200	MHz
Output frequency	FOUT	20		10000	MHz
Functional lock limits of input frequency	FREF	4		225	MHz
Output Duty Cycle, <500MHz	t_{DO}	45		55	%
Output Duty Cycle, >500MHz	t_{DO}	40		60	%
Lock Time	T_{LOCK}			100	Us
Maximum Long Term Jitter	L_{TJ}	±1% Ref Period, >=100pS			
Maximum Cycle to Cycle Jitter	C_{CJ}	±1% Output Period, >= 100pS			
Maximum Lock time		100us@5MHz			
Total Power	I_{dd}		1		mA
Static Power, when Reset is asserted and inputs are quiescent	I_{ddq}		<1		mA

31.8 Video DAC Electrical Characteristics

T_{OPT} = +25˚C, Analog power supply voltage = 3.3V, Digital Power supply = 1.2V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Dynamic Supply Current	I_{vdd}			105	115	mA
Power Down Supply Current	I_{pd}			1	5	uA
Reference Current	I_{ref}	@RSET=1.15K, REFIN=1.235V		1.07		mA
Reference Output Voltage	V_{ref}			1.235		V
Max Output Current	Io_max			34		mA
Differential Non_linearity	DLE			±0.5	±0.1	LSB
Integral Non_linearity	ILE			±1	±2	LSB
Analog Output Settling Time	Tset			10		nS
Signal-to-Noise Ratio	SNR		50	55		dB
Full Scale Error					3	%
Offset Error					3	%
Channel-to-Channel Matching Error				1		%

32 Package Dimension



SYMBOL	MIN.	NOM.	MAX.
A	1.22	1.31	1.40
A1	0.30	0.35	0.40
A2	0.92	0.96	1.00
D	14.90	15.00	15.10
E	14.90	15.00	15.10
I	1.10 REF.		
J	1.10 REF.		
M	17x17 <FULL>		
aaa			0.15
ccc			0.20
ddd			0.20
eee			0.15
fff			0.08
b	0.40	0.45	0.50
e	0.80 BSC.		
c	0.26 REF.		

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. "e" REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
3. "M" REPRESENTS THE MAXIMUM SOLDER BALL MATRIX SIZE.
4. DEMENSIONS "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM -C- .
5. PRIMARY DATUM -C- AND SEATING PLANE ARE DESIGNED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994
7. A1 CORNER MUST BE IDENTIFIED BY INK OR LASER MARK.
8. PACKAGE DIMENSIONS CONFORM TO JEDEC REGISTRATION MO–275.

Figure 32-1 Package Dimension